

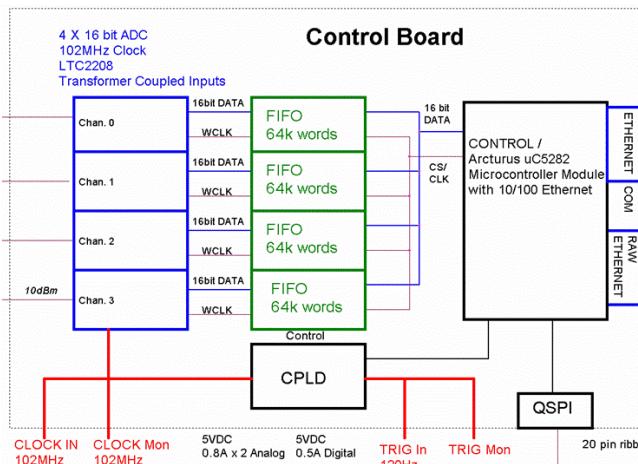
130-MHZ, 16-BIT, FOUR-CHANNEL DIGITIZER*

D. Kotturi, R. Akre, T. Straumann, SLAC, Menlo Park, California 94025 U.S.A.

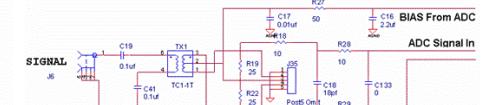
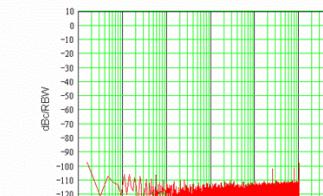
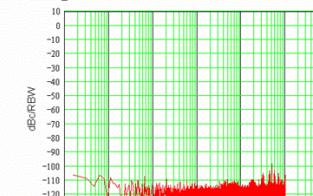
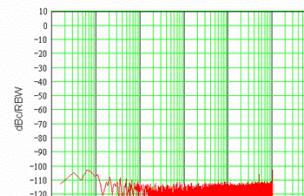
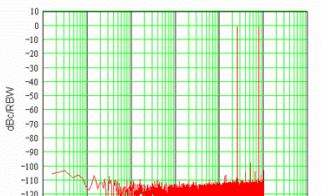
*Work supported by U.S. Department of Energy contract DE-AC02-76SF00515



↑Digitizer (shown without processor)
↓Block diagram of digitizer



FFTs of SNR for all four channels, with signal connected to one channel at a time



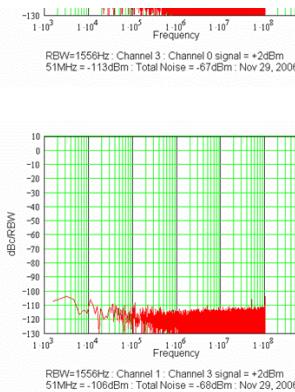
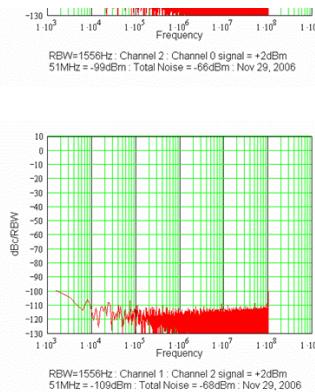
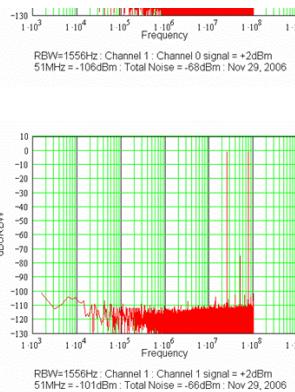
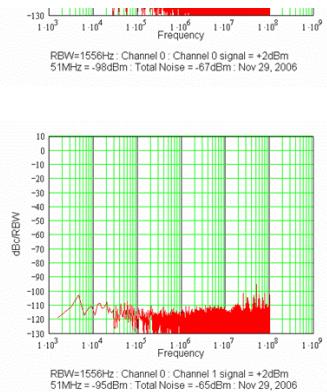
↑Input Signal

FEATURES

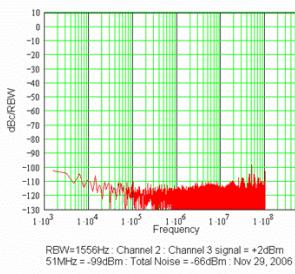
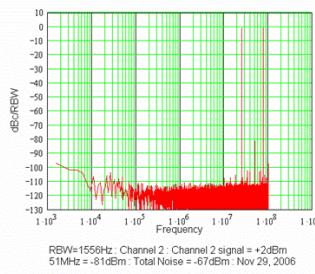
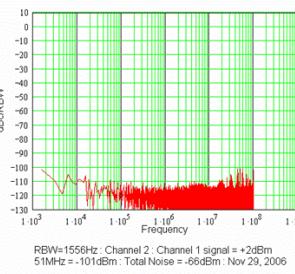
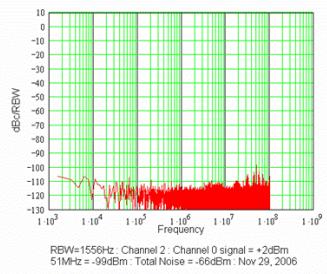
- ◎ 4 Chan - 130MSPS 16 bit ADCs LTC2208
- ◎ data clocked into 64k Sample FIFOs
- ◎ 1 buffered clock input to CPLD
- ◎ 1 buffered trigger input to CPLD
- ◎ 2 unbuffered coax I/O from CPLD
- ◎ 3 digital I/O from CPLD
- ◎ 4 interrupts to uCdimm5282
- ◎ Ethernet Port RJ45 connector
- ◎ 2nd Ethernet port using SMSC LAN9118 Ethernet Controller
- ◎ 1 COM Port to 9 pin D connector
- ◎ 1 COM Port to header
- ◎ I²C Port to header
- ◎ QSPI 4-wire Serial port with 4 chip selects to header
- ◎ 12 bit General Purpose I/O to header
- ◎ 6 10-bit MUX analog in or 4 digital I/O and 2 digital outs to header
- ◎ Software driver is EPICS R3.14.8.2+ on RTEMS 4.7.0+
- ◎ Software GUIs are edm 1-11-0m

Signal

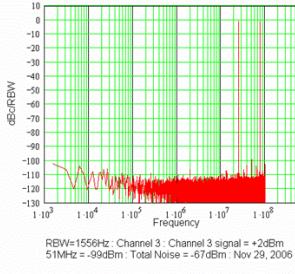
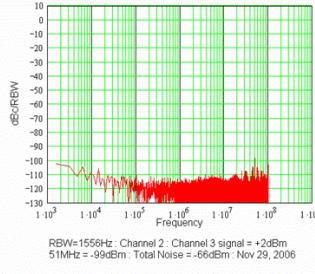
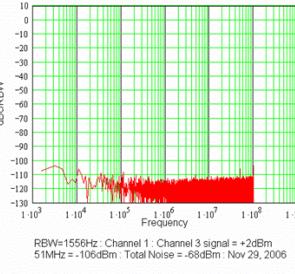
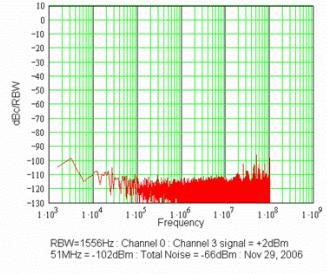
Signal in channel 1



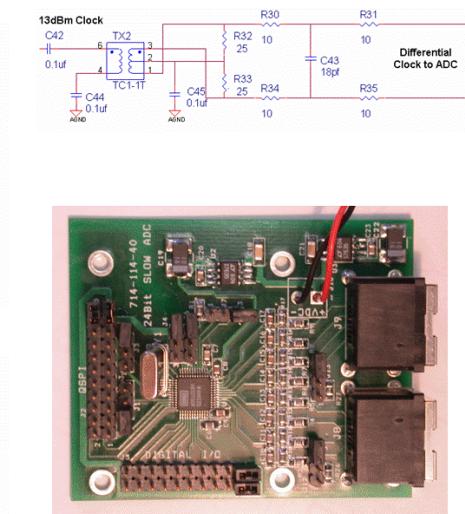
Signal in channel 2



Signal in channel 3



Clock Signal↓



↑Optional QSPI Add-on:
8-channel, 24-bit slow ADC
↓Transfer fn for the AD590

