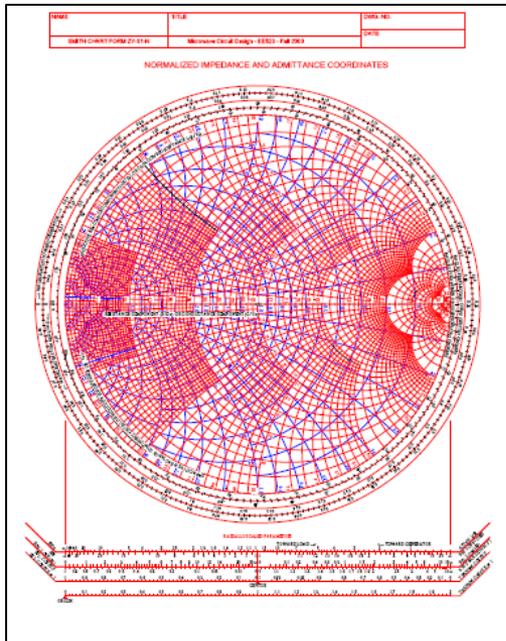
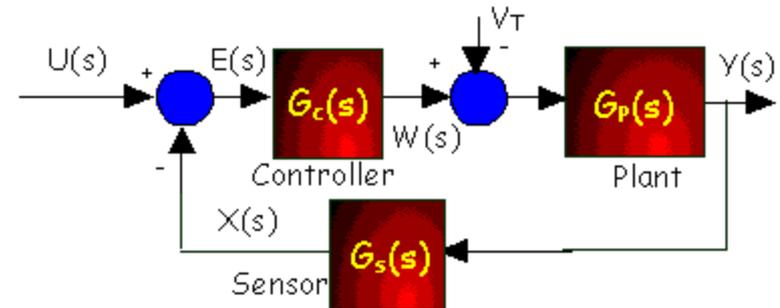


RF Happenings at Jefferson Lab



Curt Hovater



LLRF Work at JLAB

- NC VME LLRF Update
- CEBAF 12 GeV Upgrade
- RF System Overview
- LLRF System
- Resonance and Interlocks
- Packaging and Interface
- CPU-IOC
- Algorithms/Model
- Recent Tests
- Summary

LLRF People



Larry King



Trent Allison
New fatherscary



Tomasz Plawski
Likes his mixers shaken ...not stirred



Hai Dong



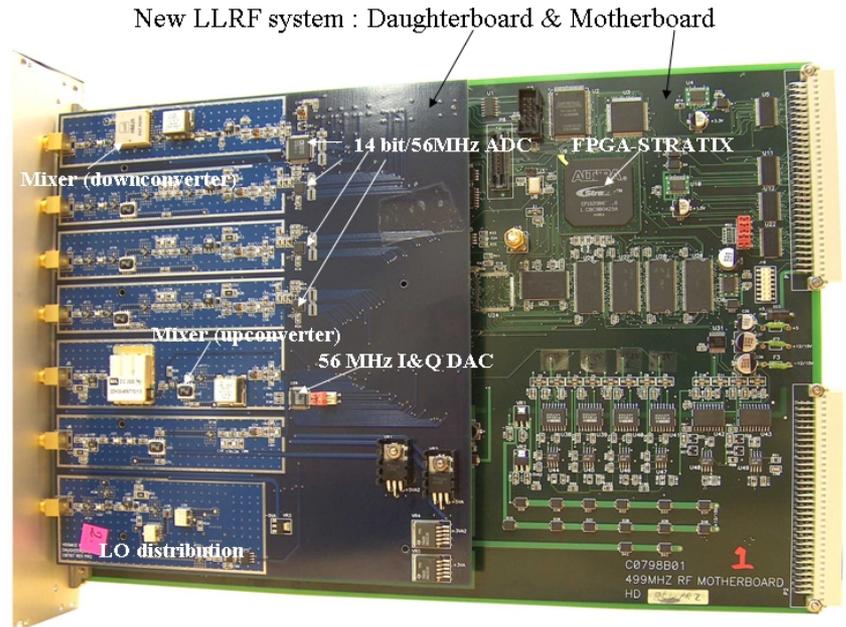
New Hire



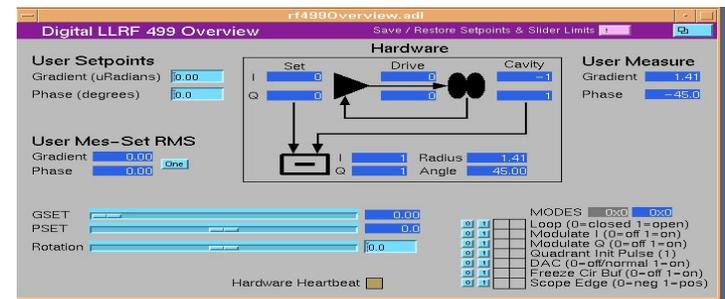
John Musson
& Rama Bachimanchi
Both on the Safety committee

Normal Conducting VME LLRF

- 13 Installed systems in three crates
- Operating since December 2005 in the injector and RF separator
- LLRF system designed around a “generic” processor motherboard
 - Motherboard uses large FPGA for PID and cavity resonance control.
 - Can support transceivers at our different cavity frequencies (499 MHz & 1497 MHz).
 - Uses GDR algorithm
 - Sleep easy operation with very little maintenance

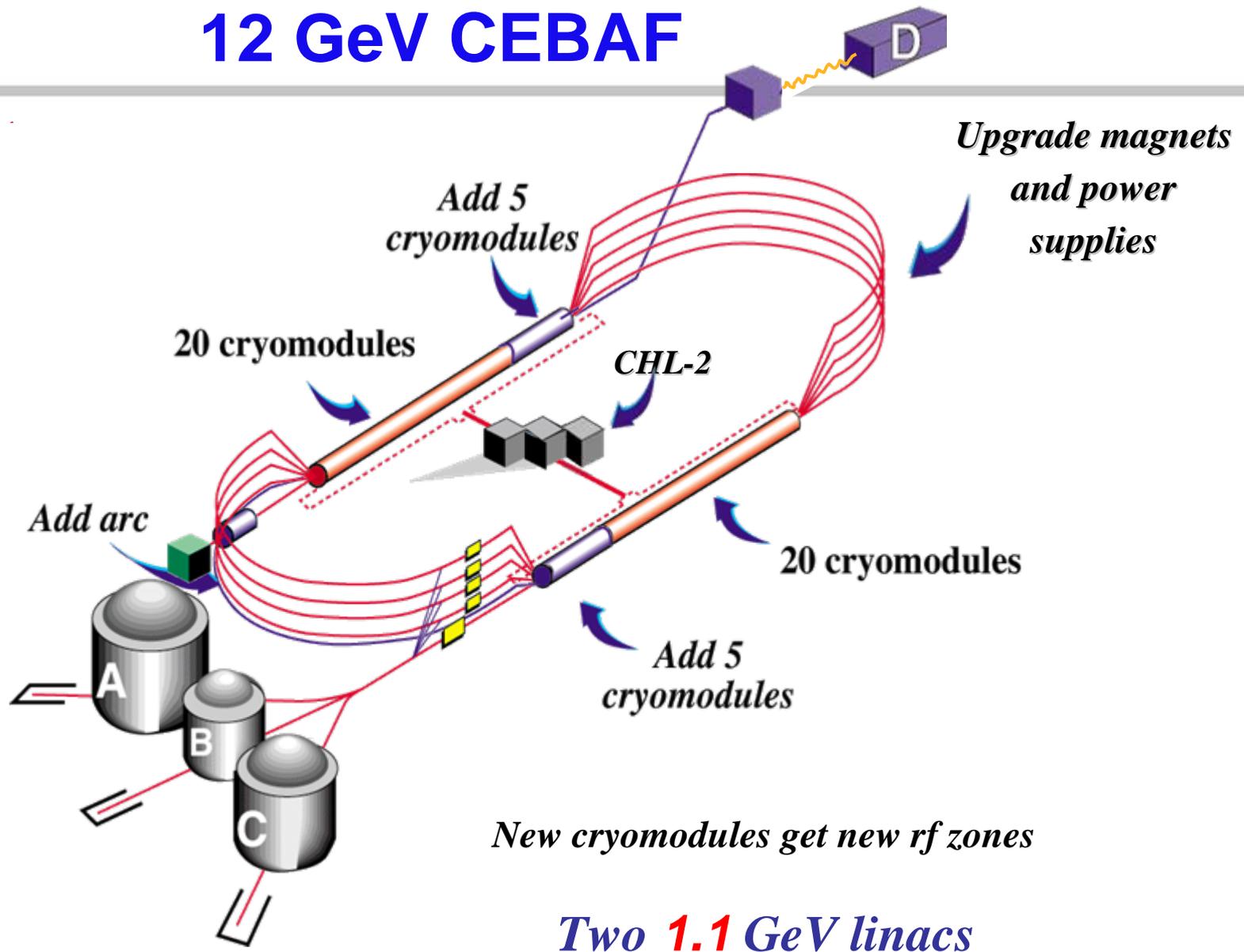


- Controlling system through EPICS



EPICS Control Screen

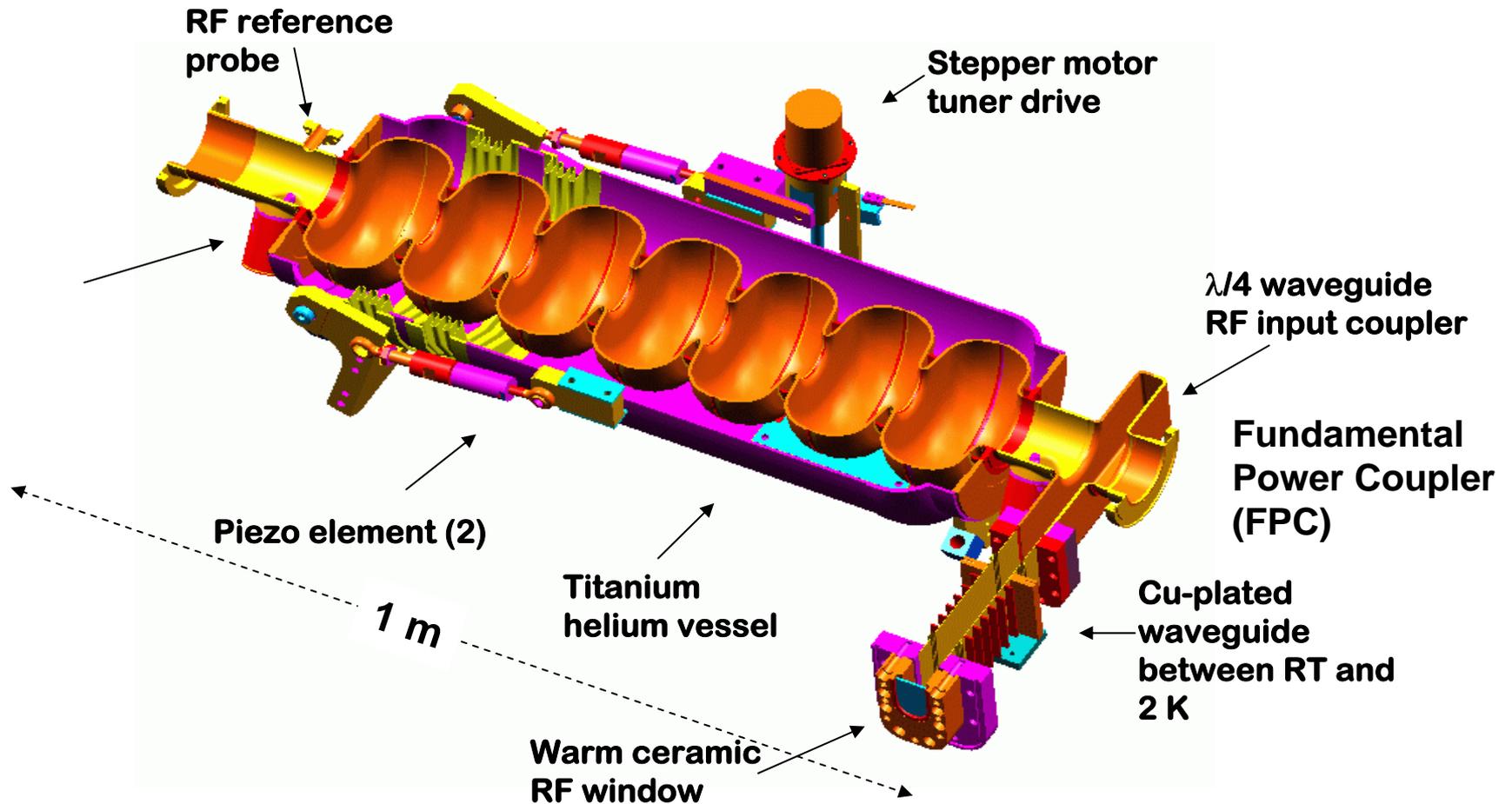
12 GeV CEBAF



12 GeV Cryomodule Parameters

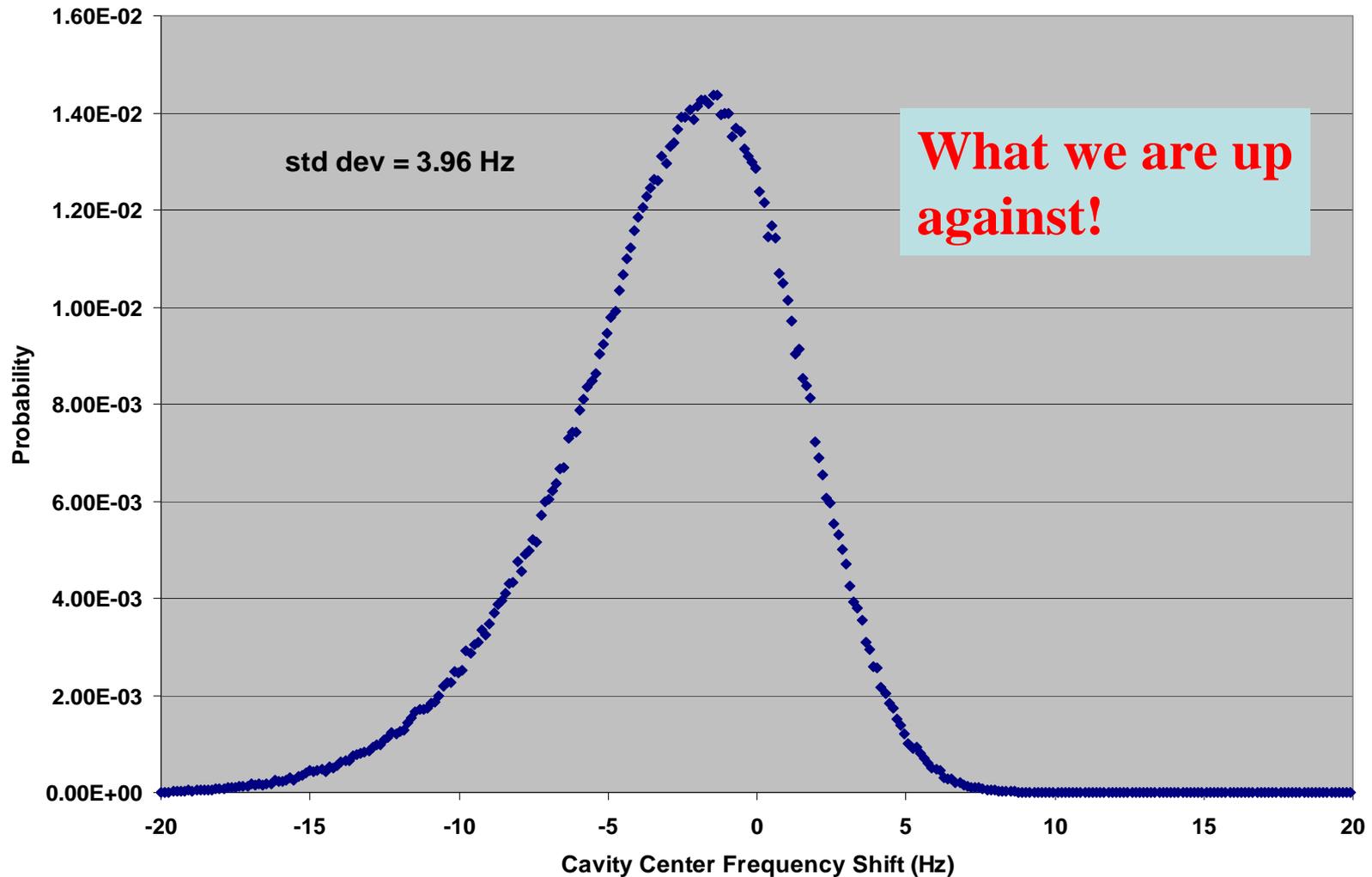
Parameter	4 GeV LINAC	12 GeV LINAC	
	5 Cell	5 Cell	7 Cell
CM Slot Length	8.25 m	8.25 m	9.8 m
Voltage/CM	20 MV	30 MV	108 MV
E_{acc} Average	5 MV/m	7.5 MV/m	19.2 MV/m
RF Windows	2	2	2
Qext FPC	6.6×10^6	same	3.2×10^7
HOM Coupling	waveguide	same	coaxial
2 K RF Heat Load	45 W	72 W	< 300 W
50 K RF Heat Load	20 W	40 W	< 300 W

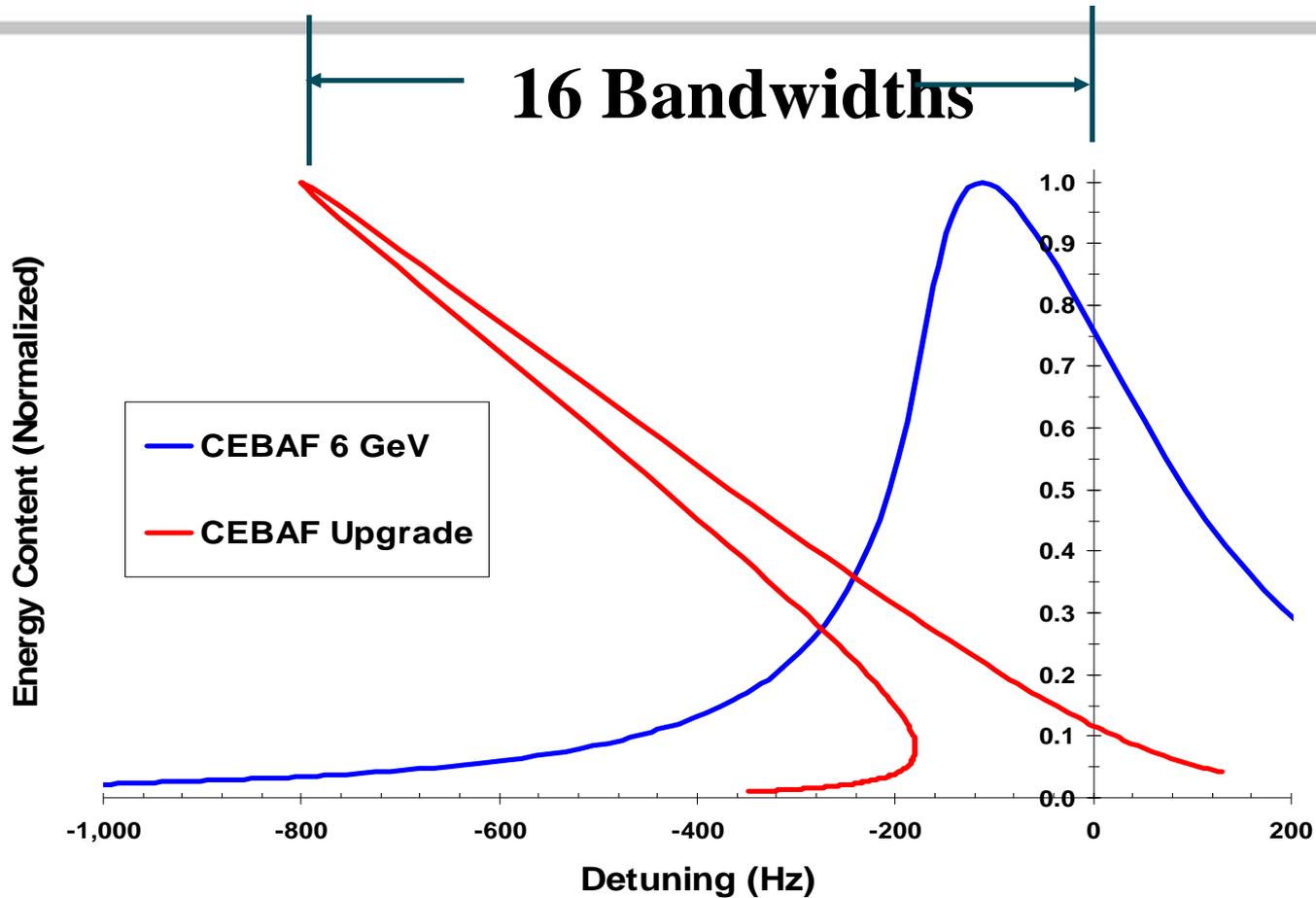
12 GeV Upgrade Cavity



HTB Background Microphonics Histogram

500k points at 1kS/sec (8.3 minutes)



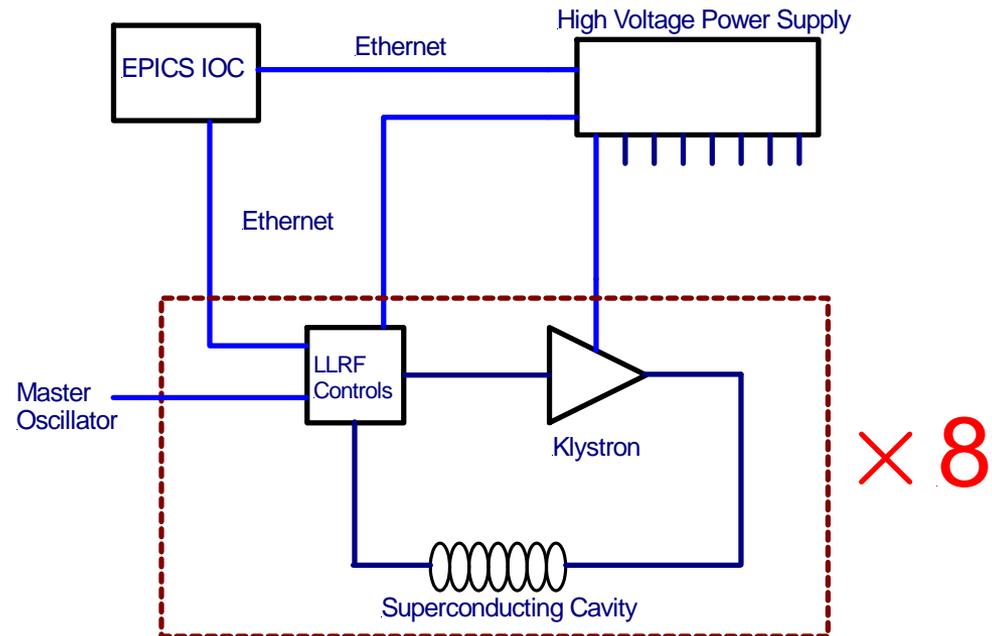


Cavity Lorentz Detuning

12 GeV RF System

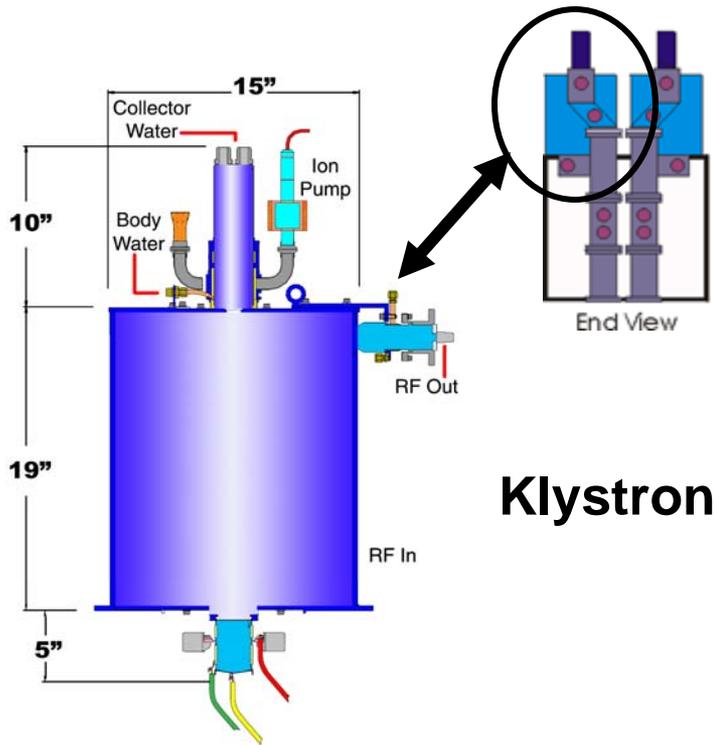
- **RF Power for 10 new zones**
 - LLRF controls for 80 cavities;
 - $Q_L \sim 3.2 \times 10^7$ (**5 times higher than 4 GeV CEBAF**)
 - **Amplitude Control Requirement – 0.045% rms**
 - **Phase Control Requirement – 0.5° rms**
 - 80 13 kW klystrons (or IOTs)
 - Waveguide components (tube to cryomodule interface)
 - 10 High Voltage Power Supplies - 17 kV/12 amps
 - Cavity tuners
 - piezo (**new for upgrade**)
 - stepper motor
 - Interlocks for cavity and RF system

Typical RF Zone

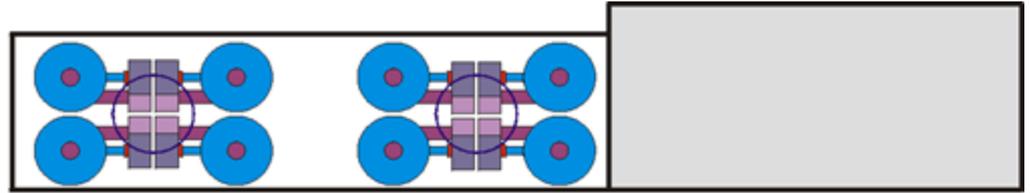


RF Power System

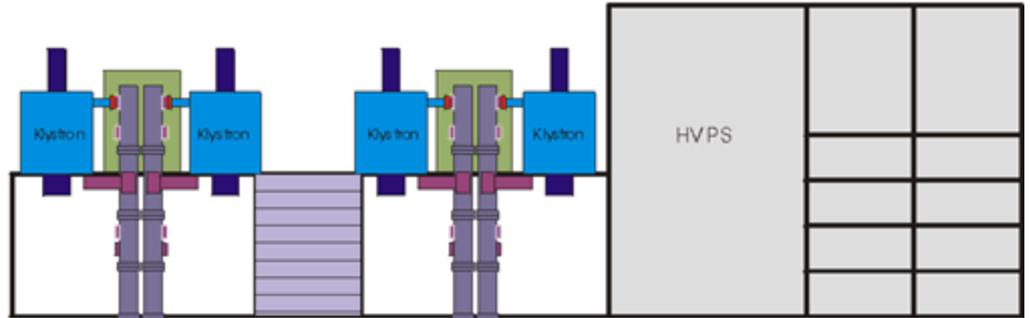
Conceptual Layout New RF Zone



Klystron



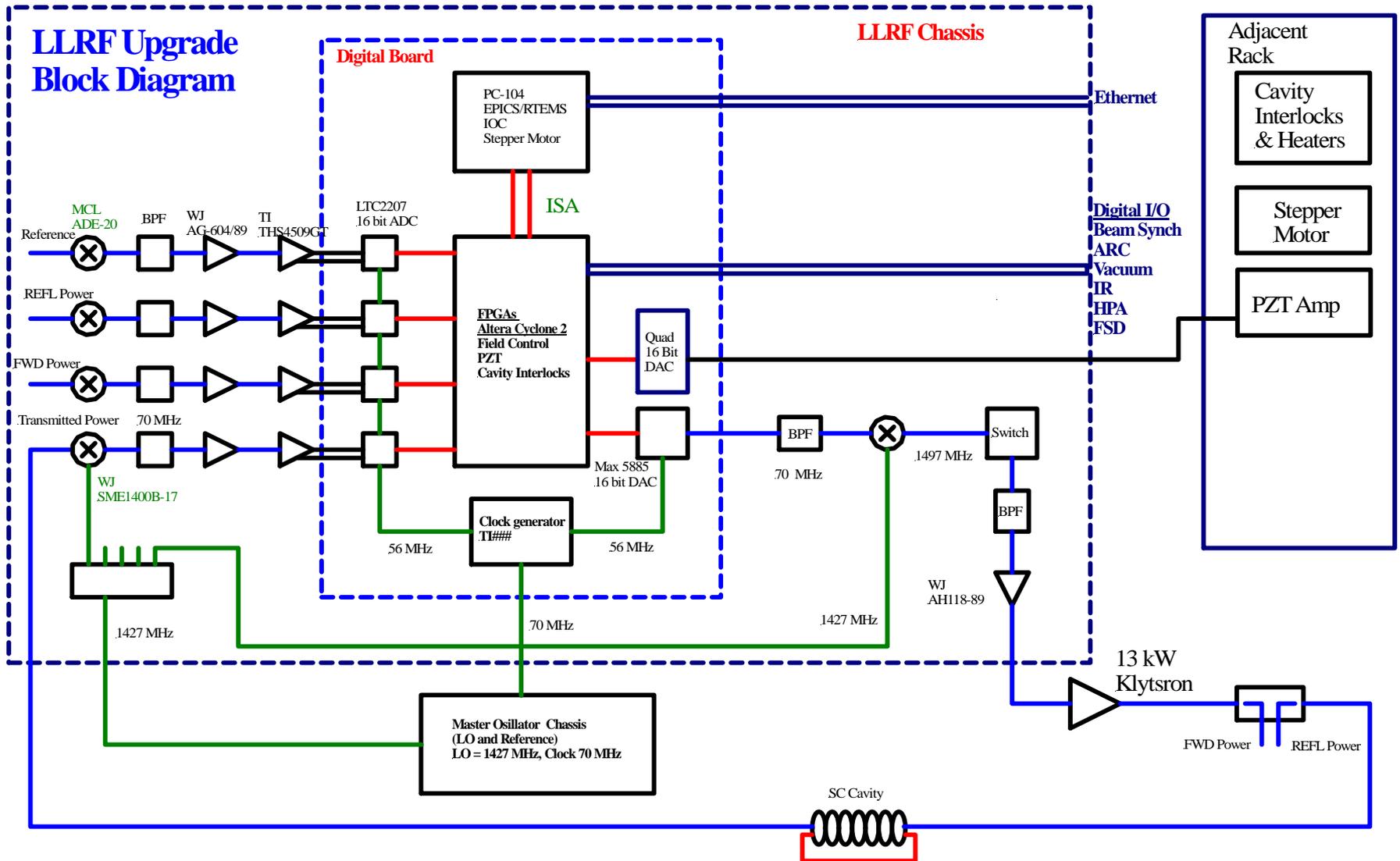
Plan View



Front View

**High Voltage PS
and Controls**

LLRF System



LLRF for 12 GeV

Design builds on our NC RF and SC prototype experience.

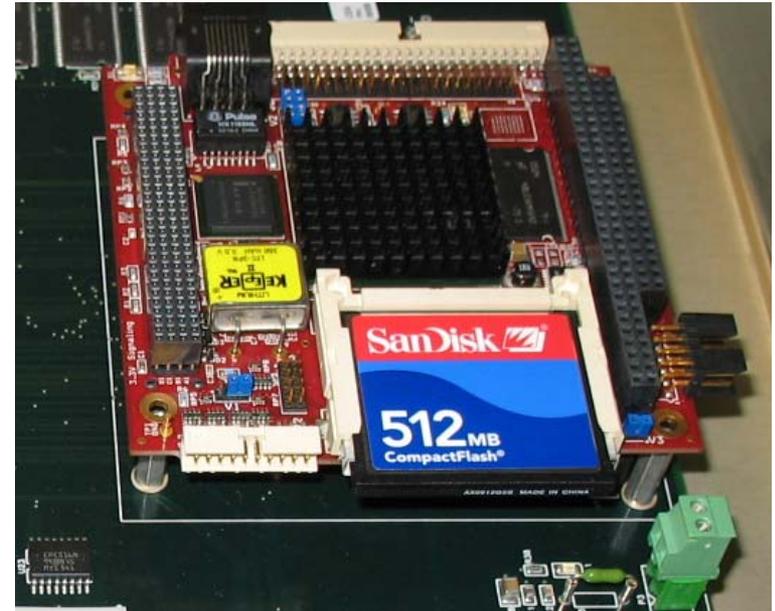
Most of the hardware concepts have been demonstrated over the last three years.

Major Improvements

- Move ADC's and DAC to digital board (noise and cross-talk improvement).
- Move towards “embedded” EPICS IOC away from VME. Design will use commercial PC-104 operating the real time operating system RTEMS.

Features

- Design allows for “Hot-swap” with minimal run-time interference.
- Hardware is algorithm independent.
- Stand Alone cavity and HPA controller
- Downloadable firmware (thru EPICS)



Versalogic Lynx PC- 104+
Installed on CEBAF
DAQ board

LLRF Field Control Chassis Components

RF Board

RF = 1497 MHz, IF = 70 MHz

- **Four Receiver Channels & One transmitter**
- **Extremely Linear front end.**

Digital Board

- **FPGA: Altera Cyclone 2 EP2C35**
- 16 bit ADC's & DAC
- Quadrature sampling at 56 MHz

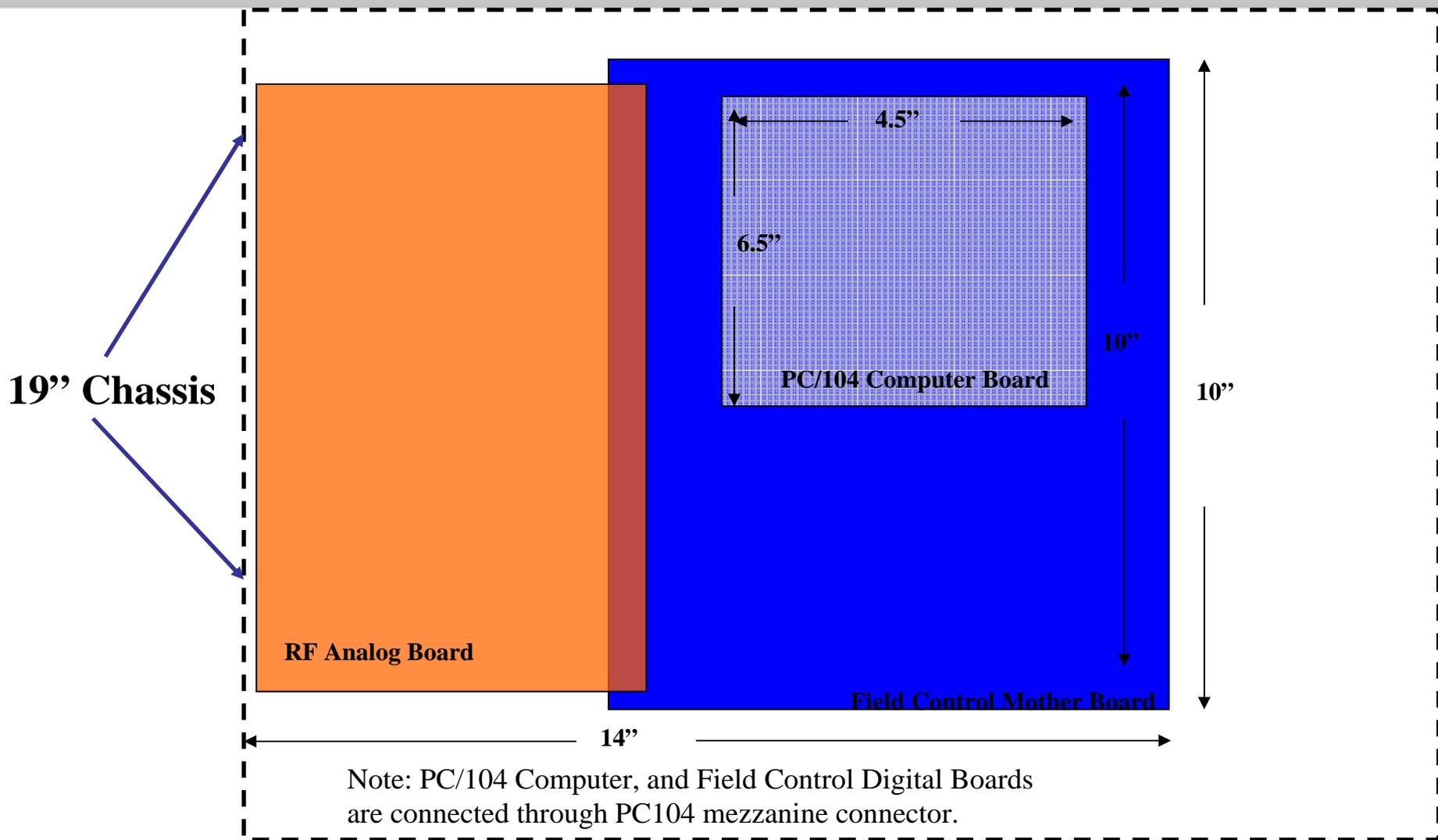
PC-104

- EPICS IOC
- **Controls Group Approved!**

Features

- Calibration and maintenance through signal loop back

LLRF BOARD STACK UP



Transceiver (4 Receive, 1 Transmit)

Receiver Specifications

Four 16 Bit ADC's

Pin: $0 \text{ dBm} < x < +20 \text{ dBm}$

$S/N > 67 \text{ dB}$ (100 kHz BW)

NF = 50 dB

C/I > 67 dB

IIP3 = + 55 dBm

Channel-to-channel isolation > 66 dB

Transmitter Specifications

One 16 Bit DAC

Pout: $-20 \text{ dBm} < x < 0 \text{ dBm}$

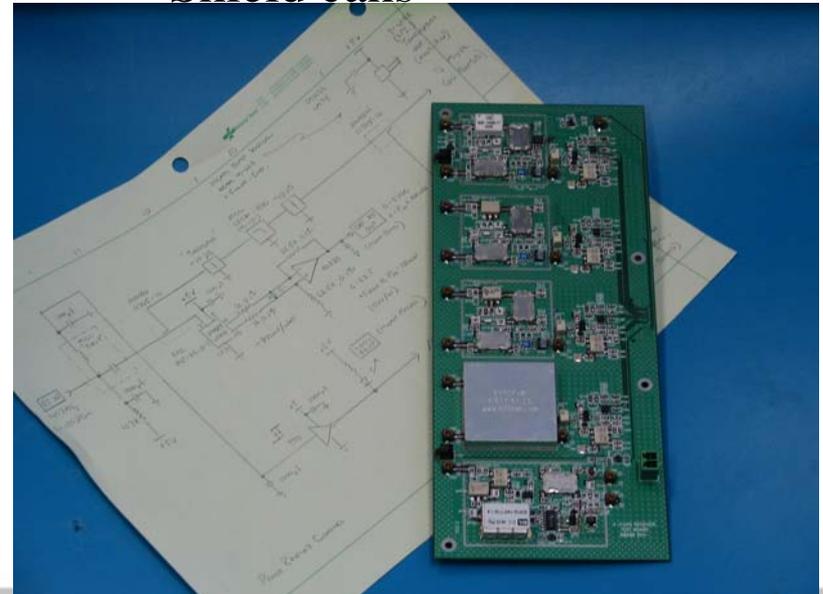
Loopback signal at + 10 dBm

TTL Tx-Inhibit

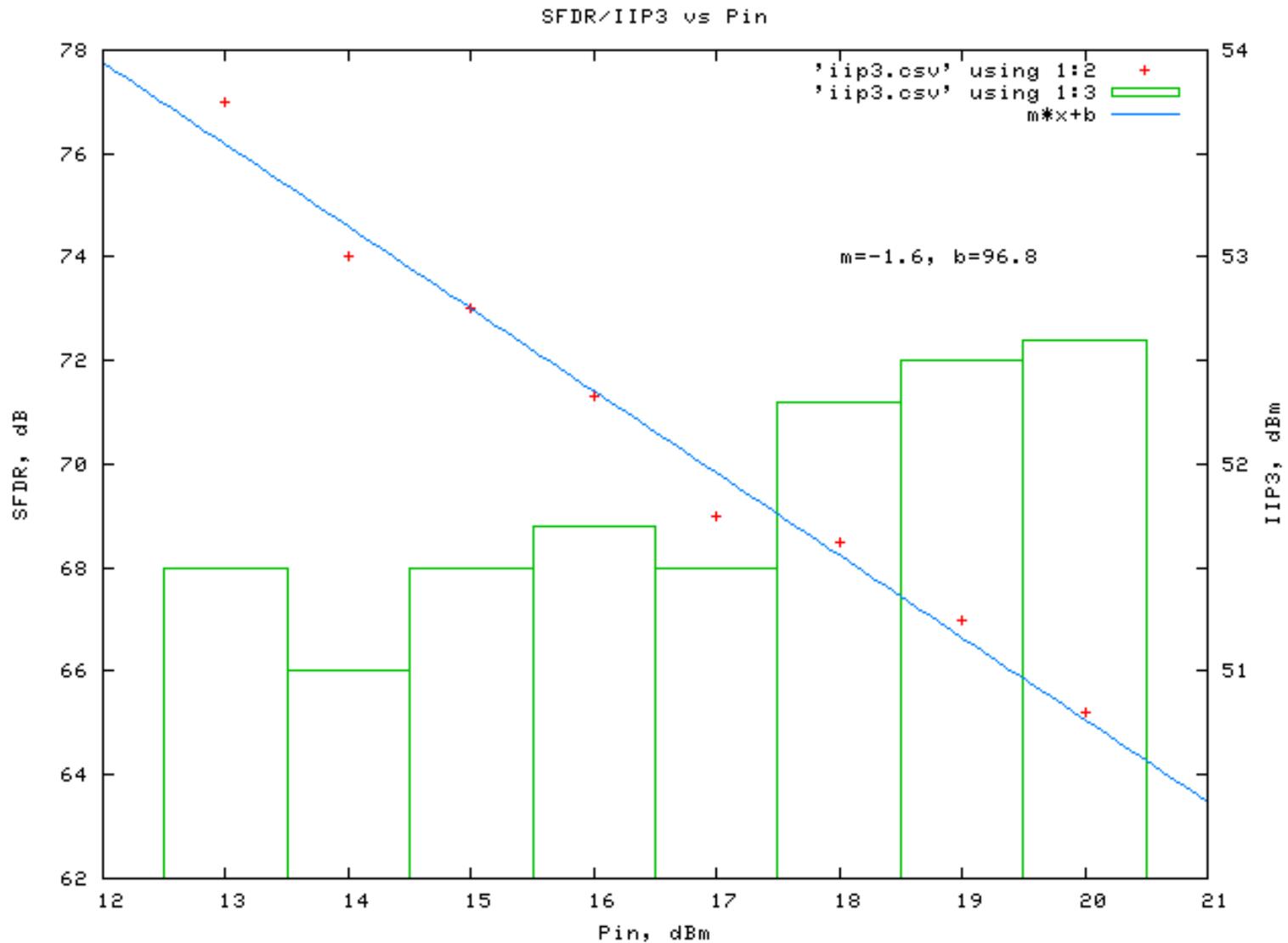
$P_{\text{diss}} = 5.0 \text{ W}$

Additional Features

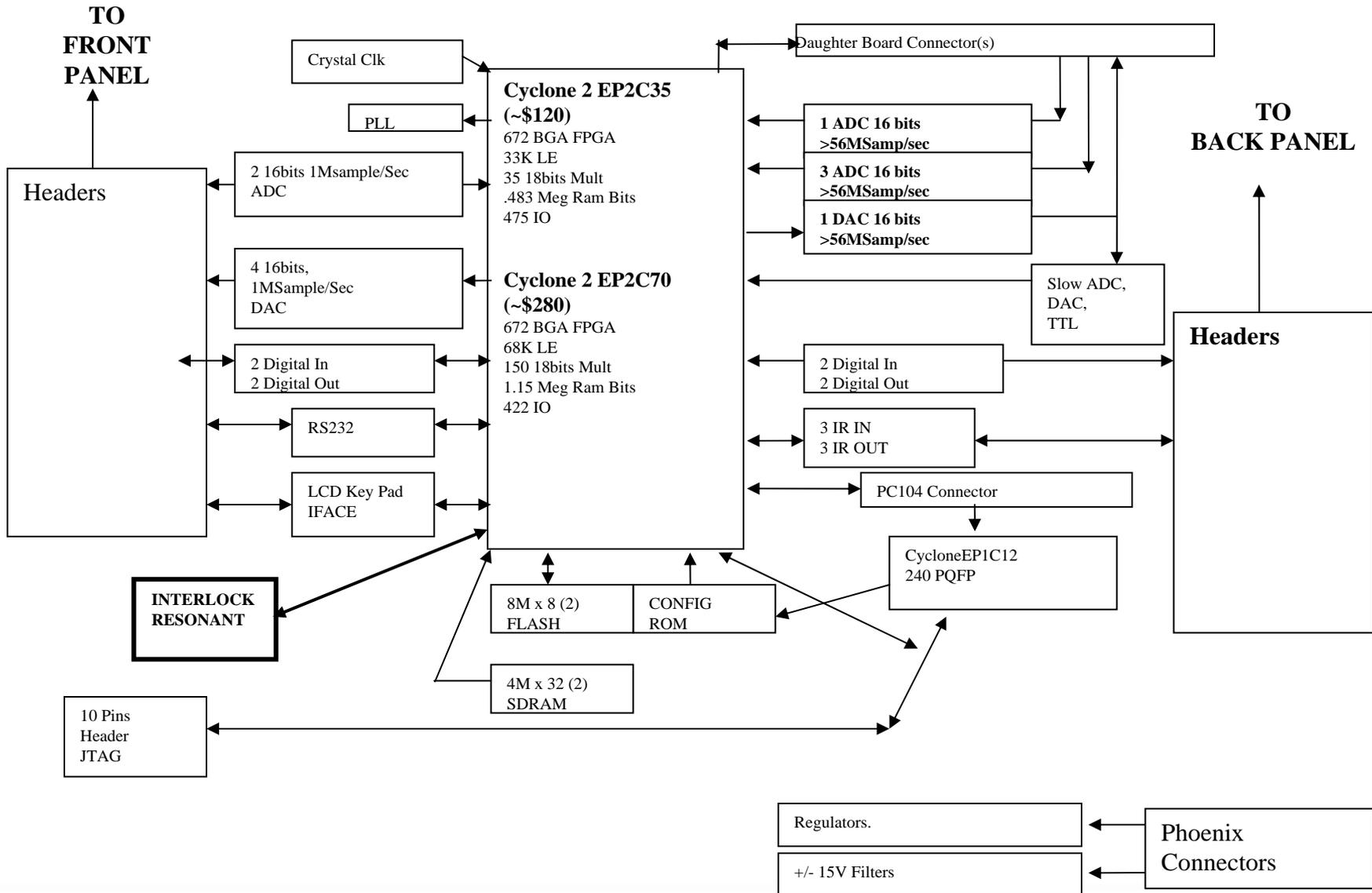
- Loopback (for calibration)
- Analog diagnostic output, proportional to Pin
- Differential IF to ADC
- Cable Fault, LED + TTL
- MMCX connectors
- Shield cans



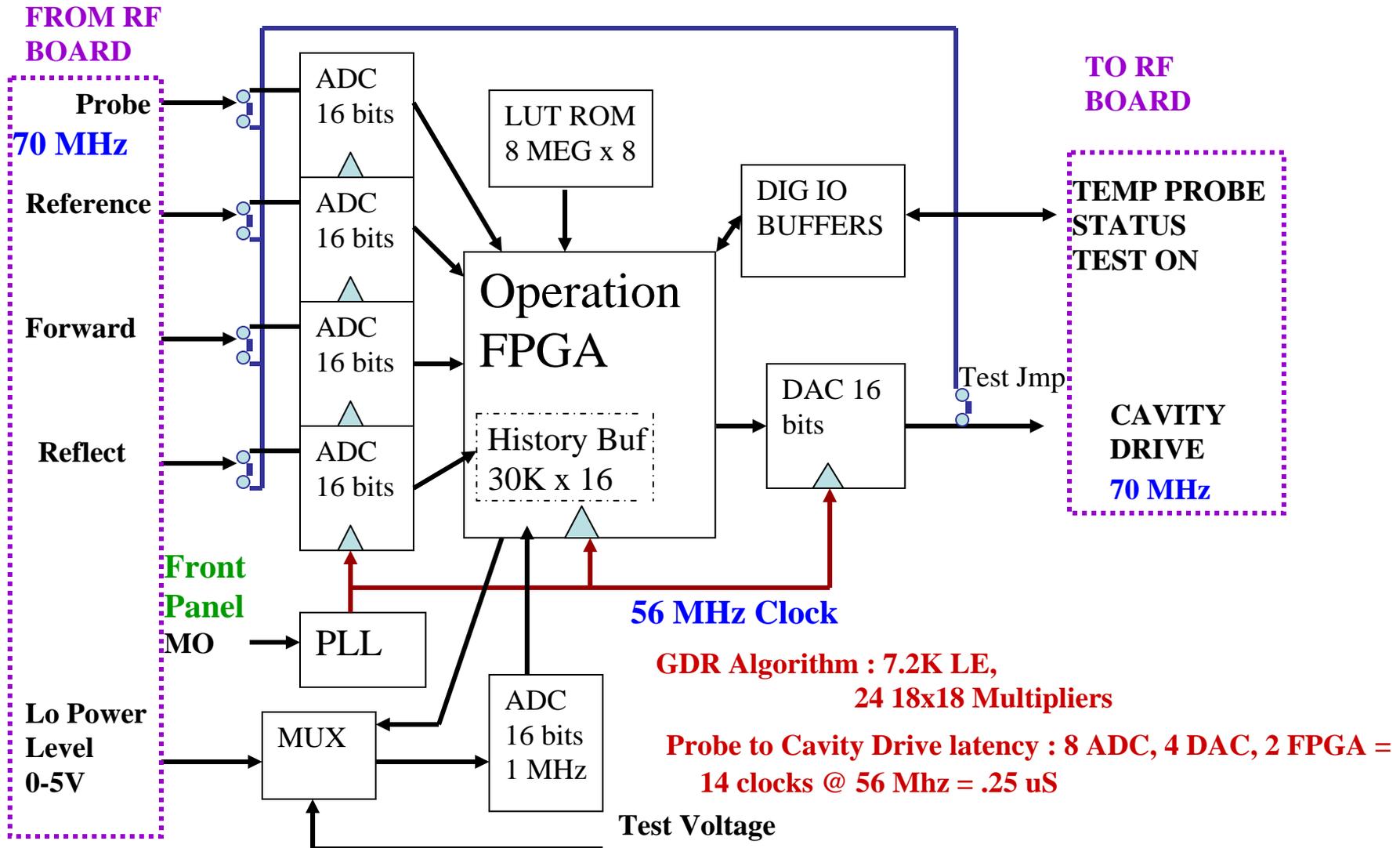
Transceiver



Digital Board Block Diagram



Field Control



Cavity Resonance & Interlocks

Resonance System

Piezo Tuner:

- Minimizes small changes in resonance due to He pressure and reduce detuning from stepper motor.
- Control logic embedded in FPGA
- Separate Chassis: one /zone

Stepper Motor:

- Recover cavity from large excursions associated with down time activities or CHL trips.
- Control software embedded in PC-104
- Separate Chassis: one /zone

Cavity Interlocks & Cavity Heaters

Interlocks:

- Arc, IR, Vacuum (waveguide & beam line), Quench, He Pressure/Level
- Separate Chassis: one /zone

Heater Power Supply

- Maintains a constant heat load in the cryomodule over various gradients.
- Separate Chassis: one /zone

Piezo Amplifier

System Specifications

- 0-150 Vdc Full scale @ 30 mA
- Bandwidth Requirements: 10 V PP at 10 Hz (sine)
- Piezo: 20 μ F &
- Stroke: 60 μ m @ 150vdc

Features

- Design uses a commercial Piezo driver :
APEX PA69
- Eurocrate format with eight
amplifiers/crate and 150vdc/200mA
supply

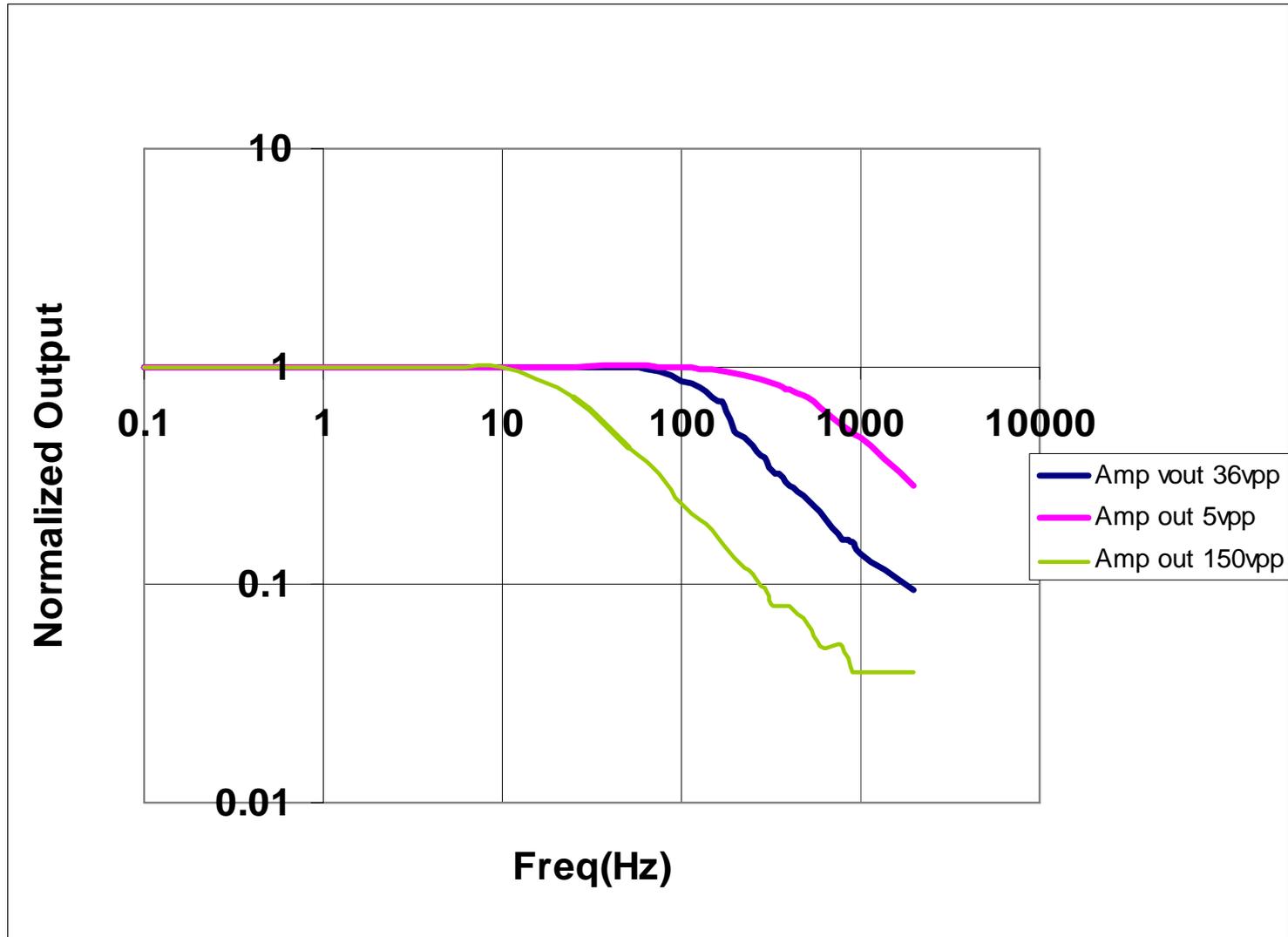
• **LOW COST!!!!**



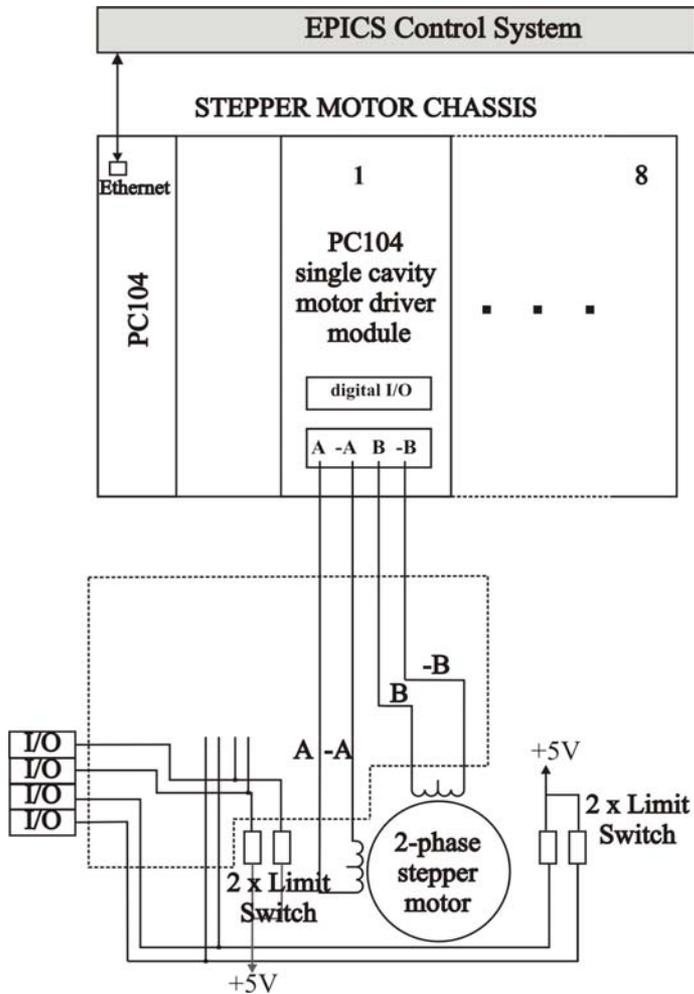
Status

- PCB has been tested on a PZT
(under load)
- Full 60 mm stroke realized @
150 vdc
- Easily meets bandwidth
requirements

PZT Transfer Function



Stepper Motor Controller



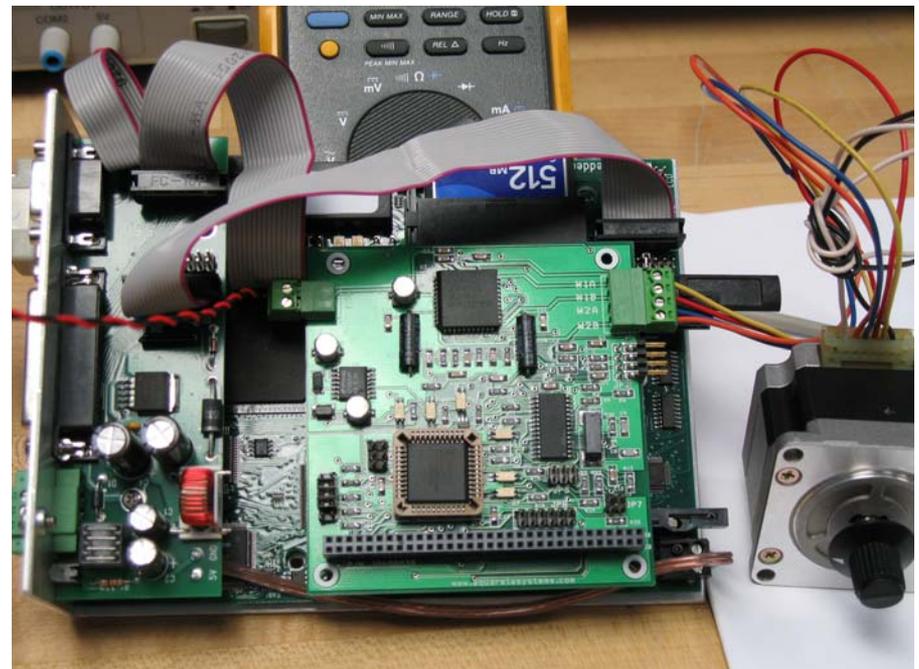
Aquarela System PC/104 characteristics:

Output Rating 35V 2.5A

Full, half, quarter and eighth step

Software adjustable chopping current limiting

Software adjustable step rate up to 12500 steps per second



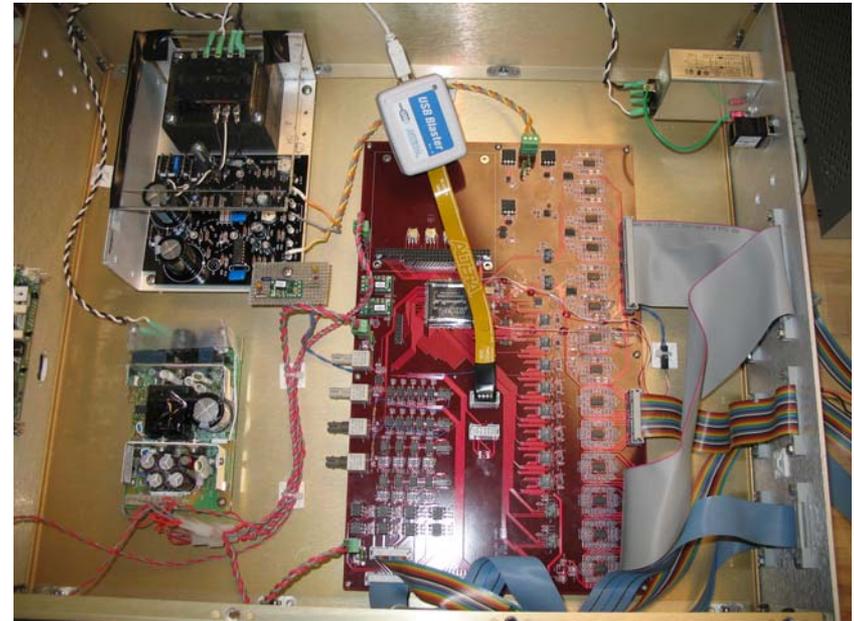
Cavity Interlocks

Features:

Continues embedded IOC theme
Using PC104 and RTEMs

Interlocks:

- Arc
- IR,
- Vacuum (waveguide & beam line),
- Quench,
- He Pressure/Level
- Separate Chassis: one /zone. i.e. interlocks 8 cavities



Prototype Chassis & Interlock board

Status: Board tested in chassis

Model and Algorithms

Model

- Incorporates main aspects of the system: cavity, klystron, and beam.

Generator Driven Resonator (GDR)

- All SC cavity tests have been completed using a GDR
- Prototype PZT and Stepper Motor Algorithms have been successfully tested (Alicia Hofler).

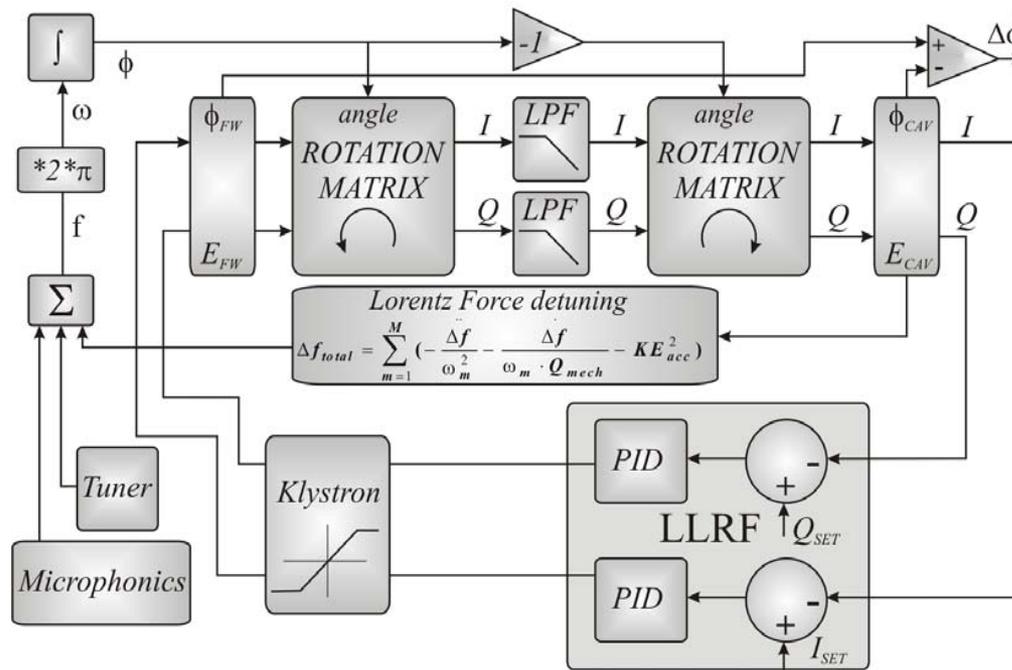
Self Excited Loop (SEL)

- Algorithm is being developed. Bench Tests completed.
- Cavity tests showed digital SEL works very well
- Incorporation of Phase and amplitude control on going
- **See John Musson's Talk Tuesday Morning**
- **Final Design will incorporate an SEL**

Cavity Control Loop Simulink Model

Model highlights

- Practically DC simulation therefore fundamental sampling time for processing can be large (~1usec) thus simulation speed is high.
- Two low pass first-order filters with cutoff frequency = cavity bandwidth/2
- Rotation matrix for quadrature components to reflect detuning frequency
- Lorentz Force Detuning : second order differential equation reproduces mechanical modes of cavity
- Microphonics: External noise generator



Cavity phase and gradient during 4.3 Hz RMS background microphonics



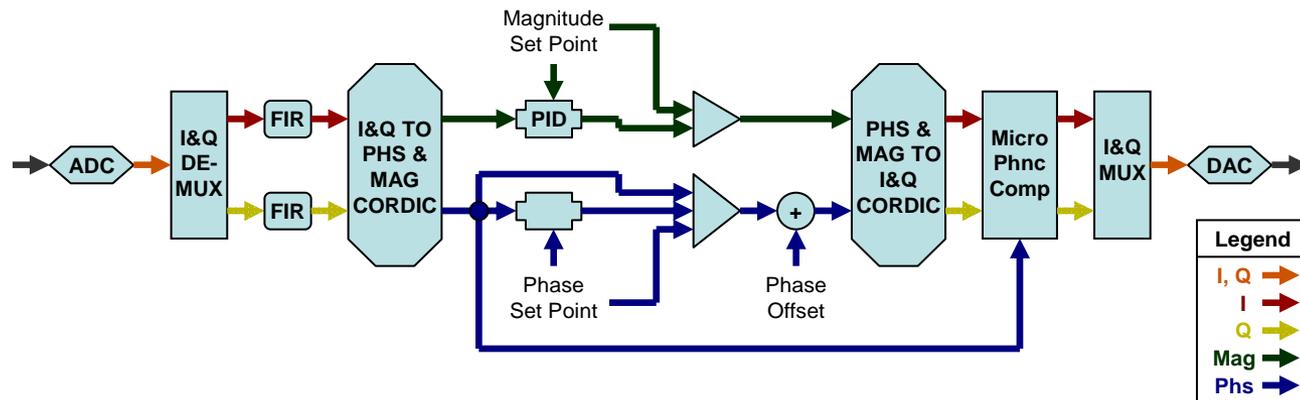
Loop gain $P=80$, $I=0$ $\Delta \text{field}_{\text{RMS}}=0.0004\%$ $\Delta \text{phase}_{\text{RMS}}=0.13^\circ$

Algorithm Independent Hardware

Hardware has been tested using a GDR and SEL algorithm.

SEL allows for rapid resonance capture. Field control bugs still being massaged.

GDR field control easily met specifications.



SEL Block Diagram

12 GeV LLRF Packaging

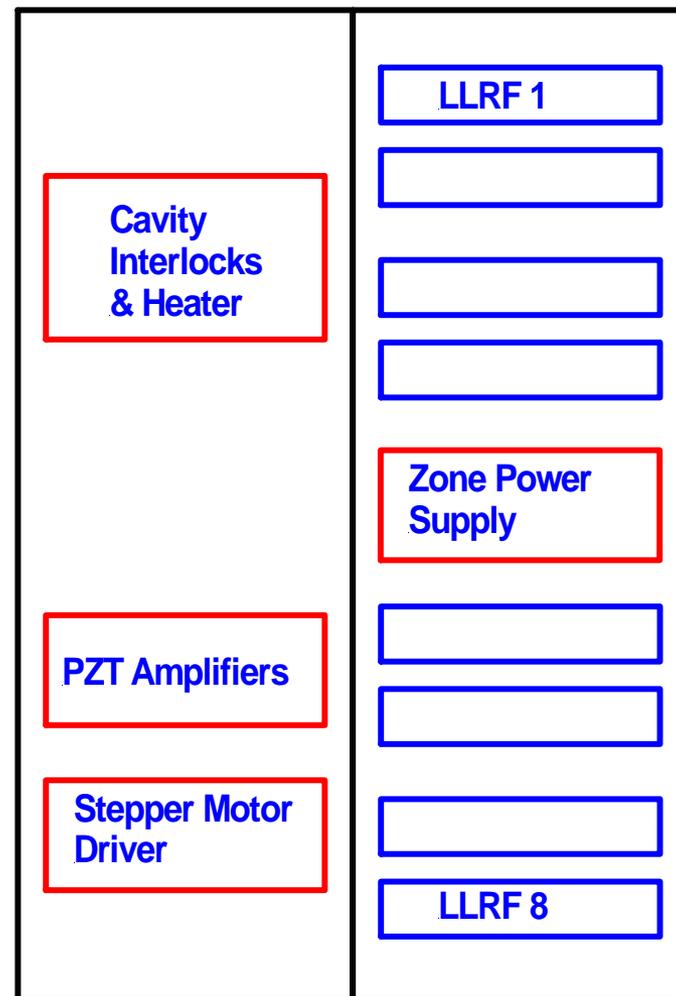
Eight LLRF controllers in one rack

- Each with a 2U Chassis

Adjacent rack contains

- Stepper motor drives
- PZT amplifiers
- Cavity interlocks
- Cavity Heaters

LLRF Racks



2008/9 Design Tasks

Field and Resonance Control validation

- Complete Digital Board testing
- Test hardware, field control and resonance algorithms on upgrade cryomodule in CEBAF or FEL

HPA Control

- Logic Based controller. Allows the HPA to be a stand alone unit.
- Status: AIP project ongoing to retrofit existing HPAs. Has been tested in and idle zone in CEBAF.
- Even though New HPA has yet to be designed we believe the system can be designed as a generic controller.

Master Oscillator & Distribution

- The reference distribution needs to be extended five zones in the NL and fitted with five couplers in the SL.
- Status: This task is a 6 GeV Accelerator Improvement Project.

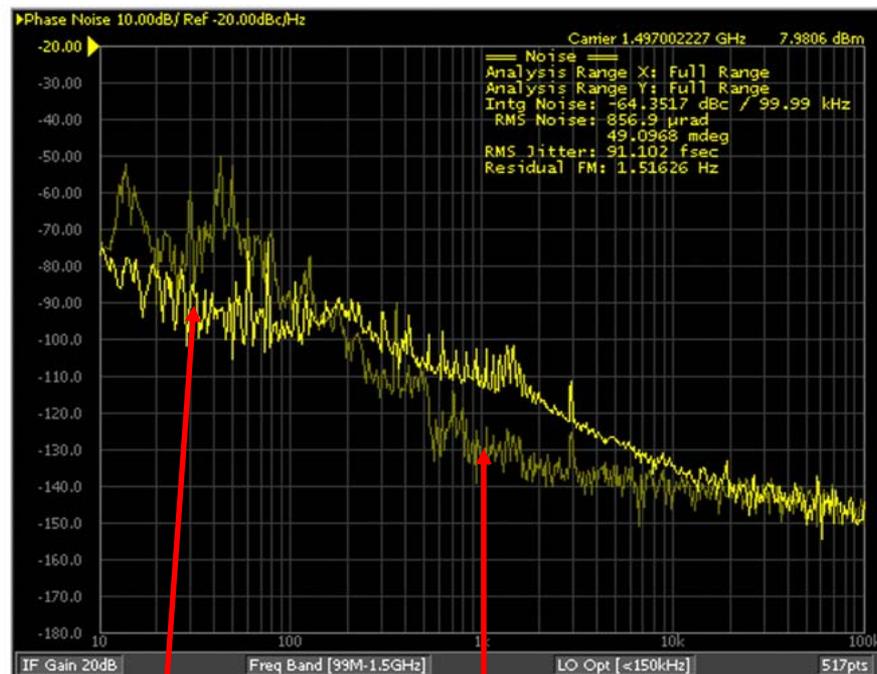
LLRF Test Stand

- To be developed in 2008 as the first LLRF prototype chassis is undergoing testing.

LLRF Cavity Measurements

Phase Stability

- Easily Met 12 GeV specification 0.5° rms. at ~ 17 MV/m
- Typical phase error was $< 0.05^\circ$ rms. (91 fs)* after gain optimization at 1497 MHz.
- Phase noise dominated by the master oscillator LO reference $\sim 0.05^\circ$ rms. (96 fs)* at 1427 MHz.



Closed Loop

Open Loop

LLRF Phase Noise

* Statistical error of SSA

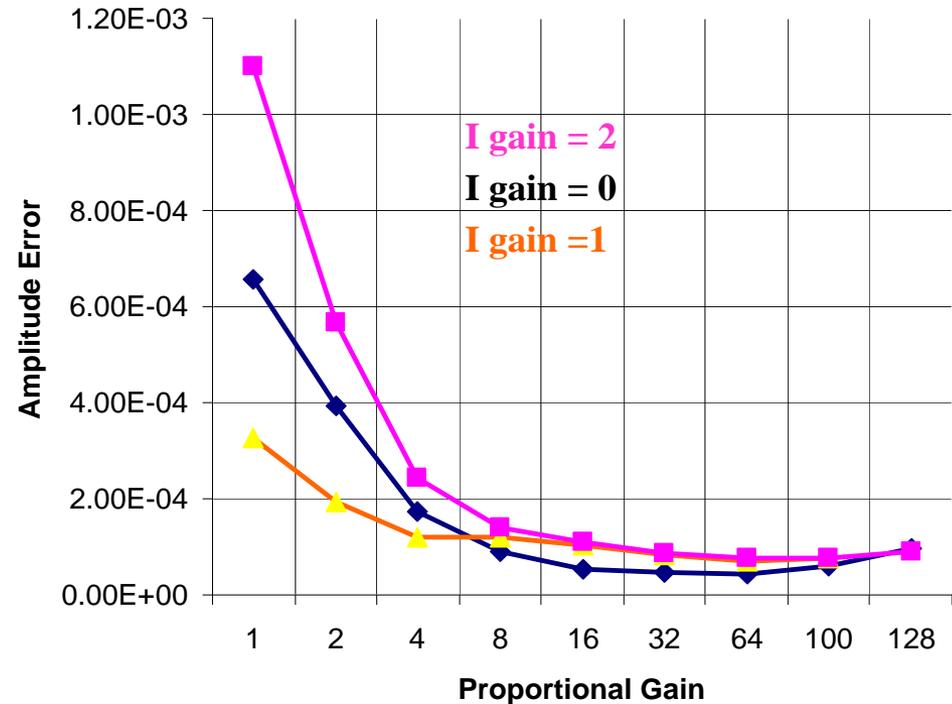
LLRF Cavity Measurements

Amplitude Stability

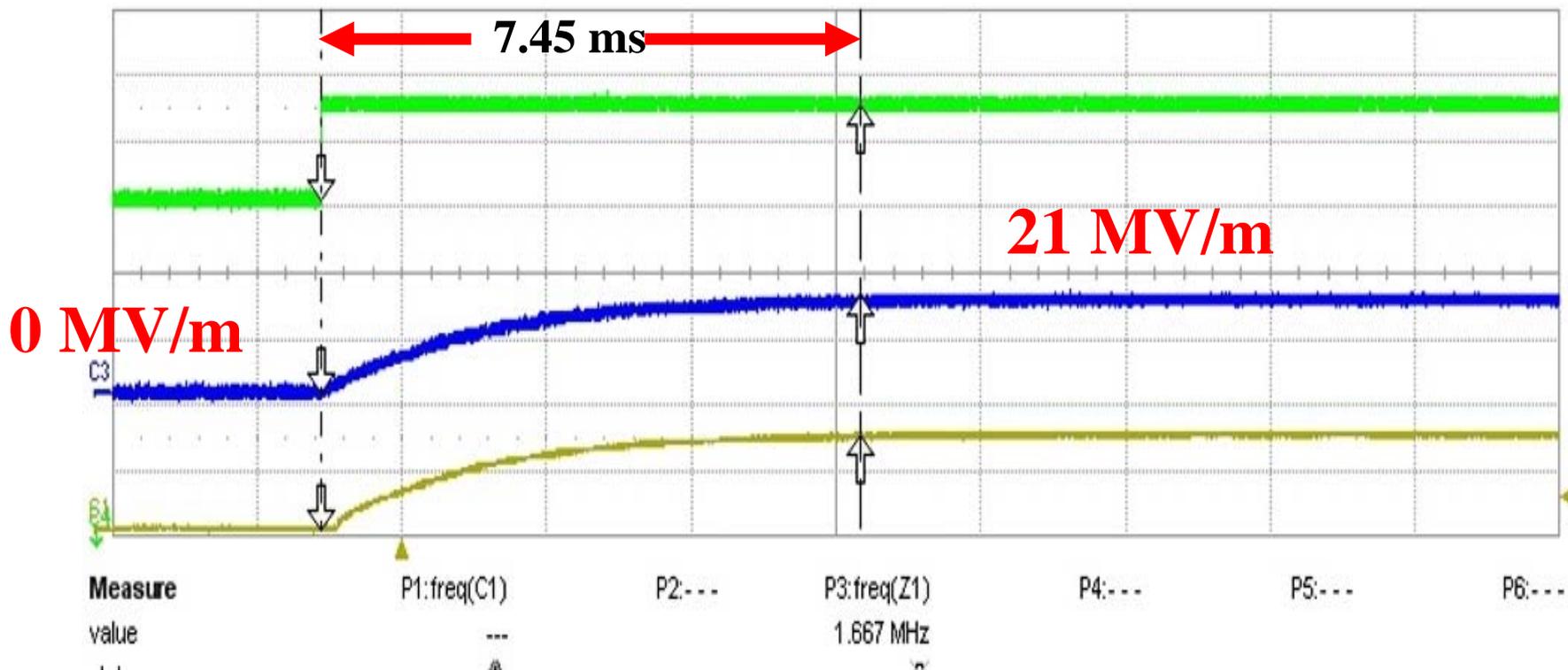
- Easily met amplitude specification 4.4×10^{-4} at 17 MV/m
- Typical amplitude error after gain optimization is $< 5 \times 10^{-5}$
- Present upgrade cryomodules very microphonic quiet* 6 Hz (6σ) compared to CEBAF 20 Hz (6σ)
- Therefore proportional gain needed is small < 30

***New cryomodules will not have stiffening rings. Expect microphonics to increase and the required gain to increase also.**

Measured Amplitude Error vs. Proportional Gain



SEL Tests on Upgrade Cavity



Cavity recovery using digital SEL. 0 to 21 MV/m in 7.45 ms!

Green Trace control output from LLRF,

Blue Trace Calculated GMED via LLRFCM, Yellow Trace Diode signal from cavity.

Summary

VME Based systems are operating with no complaints

12 GeV LLRF is progressing well

- RF Board Tested. Digital Board being manufactured
- PC-104: EPICs running on top of RTEMS
- Resonance and interlocks: PZT System design and tested, Interlock chassis design and tested
- Interface and Packaging is investigating ways to make it easy for assembly, installation and maintenance

R&D testing

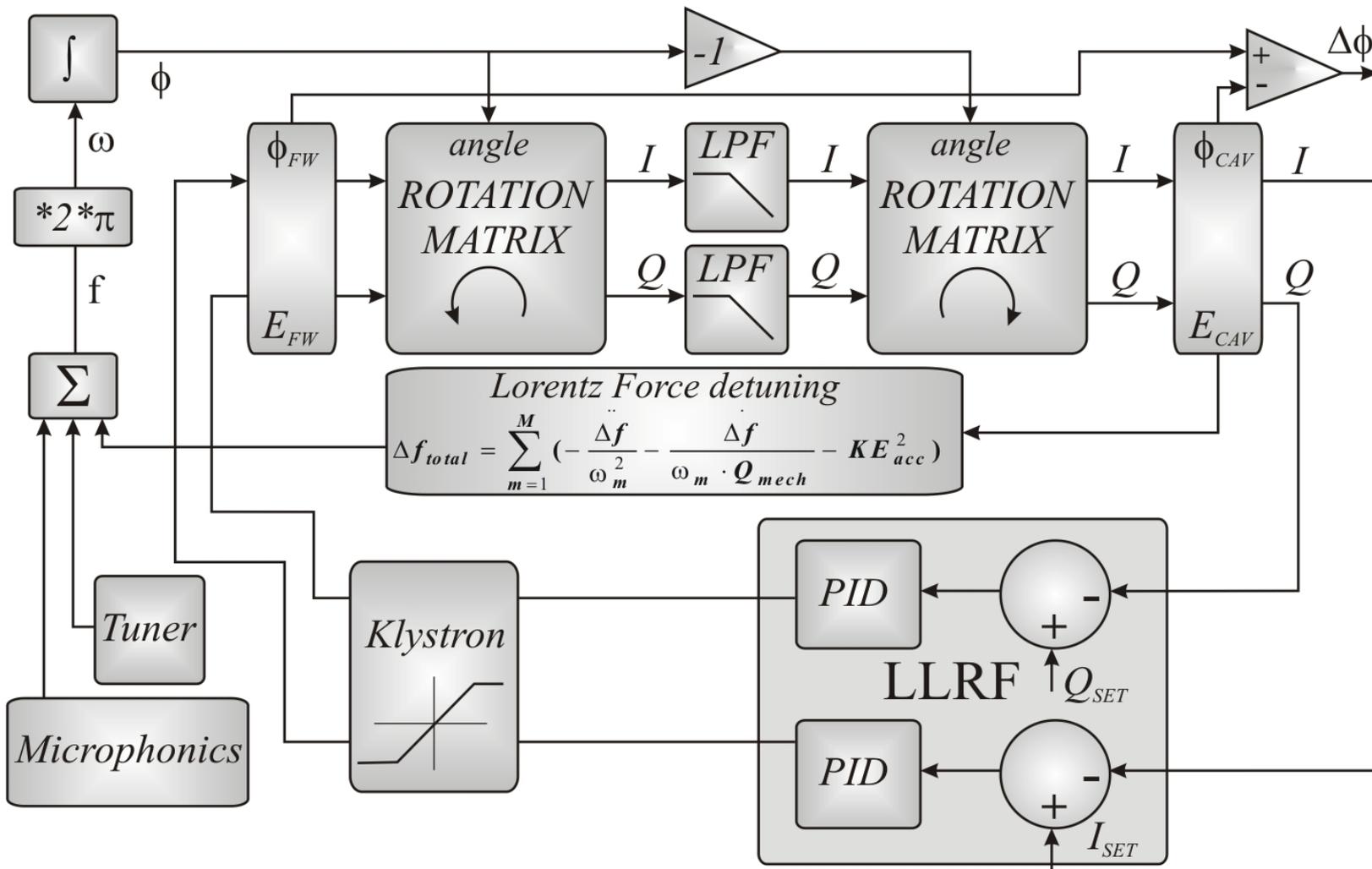
- All field control specs have been met to 21 MV/m.
- Operational expectations/requirements to be tested before 12 GeV shutdown.

Algorithm Development

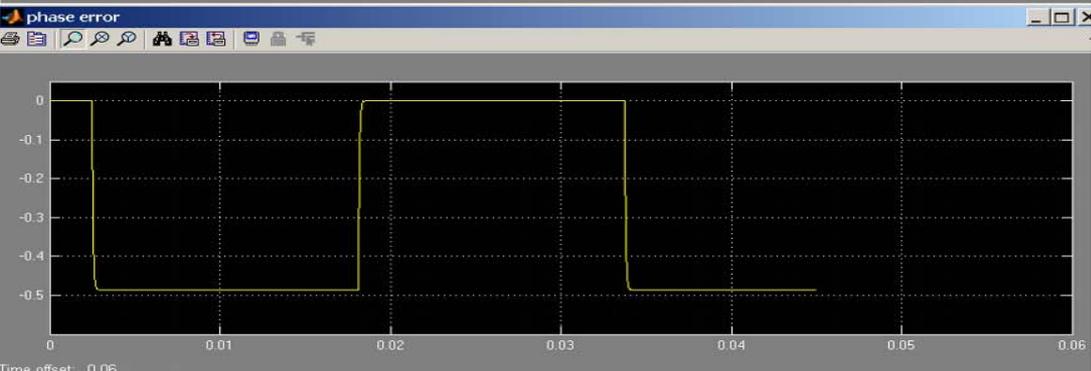
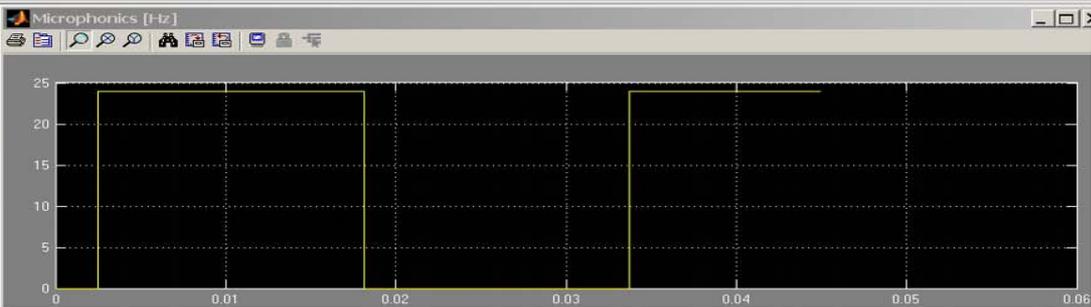
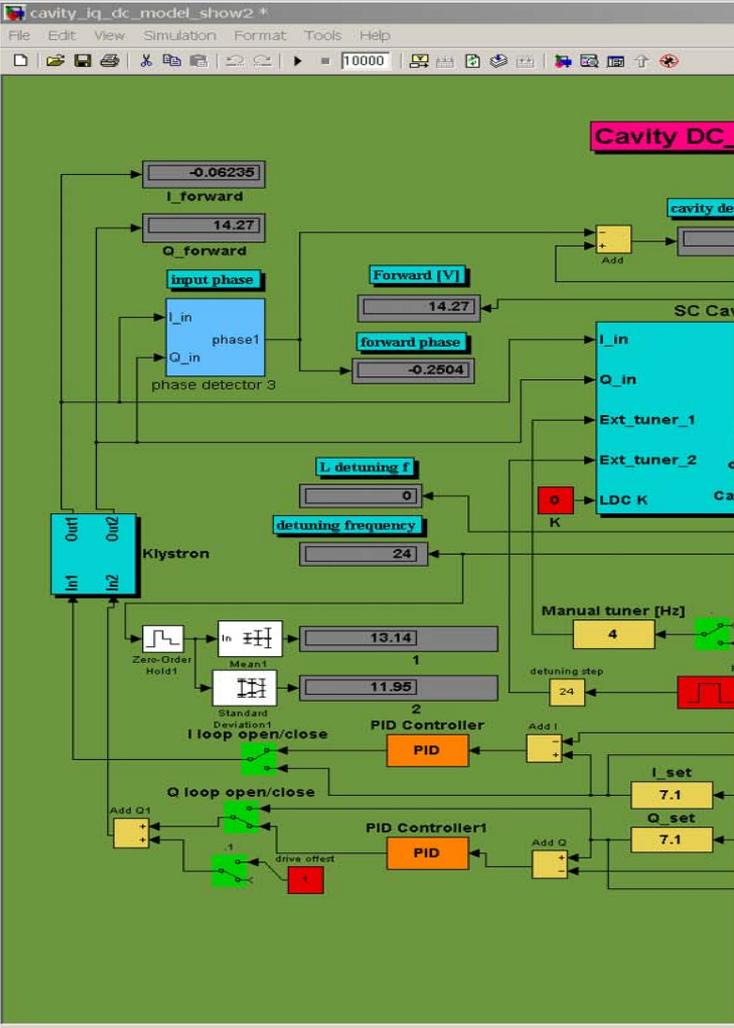
- SEL: Tested on cavity to 21 MV/m
- Operational Algorithms (Tuning, calibration etc.) on track. Hardware/software can accommodate all requirements.

The Cavity Control Loop model has been developed for analyzing the basic aspect of control system. Typically complex cavity representation is simplified to quadrature components crossing low pass filter outline by cavity bandwidth. Lorentz Force detuning, microphonics and tuners function are incorporated as a frequency modulators.

Block diagram of cavity control loop model

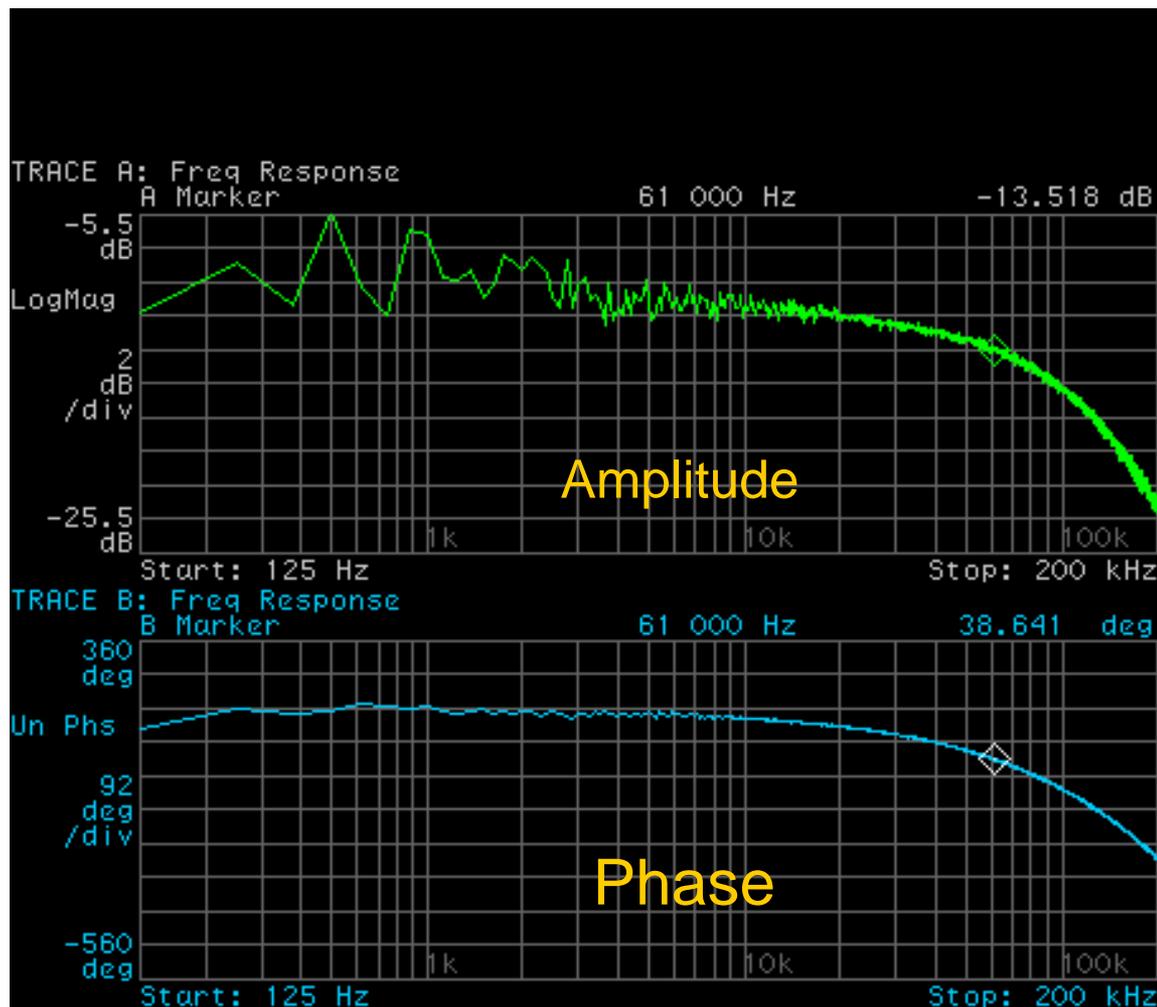


Cavity phase and gradient with 24 Hz (6 σ) step detuning distortion



Loop gain $P=120, I=0$ Δ field=0.003% Δ phase=0.48 deg

Control System Bandwidth ~ 60 kHz



12 GeV Upgrade Status & Schedule

- **Critical Decision 0 (CD-0) approval March 2004**
- **CD-1 approval in February 2006.**
- **Preliminary engineering design work started (physics and accelerator).**
- **Lehman Review in June 2007**
- **On track for CD2 in November 2007.**
- **Construction to begin in first 1/4 FY 2010**
- **Installation: 2011 (during an extended CEBAF maintenance down)**
- **Accelerator Commissioning: mid 2013**