



# A Fully Integrated Controller for RF Conditioning of the LHC Superconducting cavities

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# Outline

- Conditioning
  - Definition
  - Requirements
  - Classic Method
- Analog Conditioning System
- LHC SC RF Conditioning
  - Motivation for a new digital system
  - Implementation
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    - New Digital System vs Initial Solution
    - Conditioning DDS Module
    - Design Flow and Management
- Software Architecture
  - Overview
  - Real-time operation
  - LabView Application
- Conclusions

# Definition

## ■ Conditioning

*“a learning process in which an organism's behavior becomes dependent on the occurrence of a stimulus in its environment”*

- RF conditioning – Bringing field and power to nominal levels by a vacuum controlled training process
- Periodic RF Cleaning needed to maintain cavity performance
- A.k.a. power and field processing

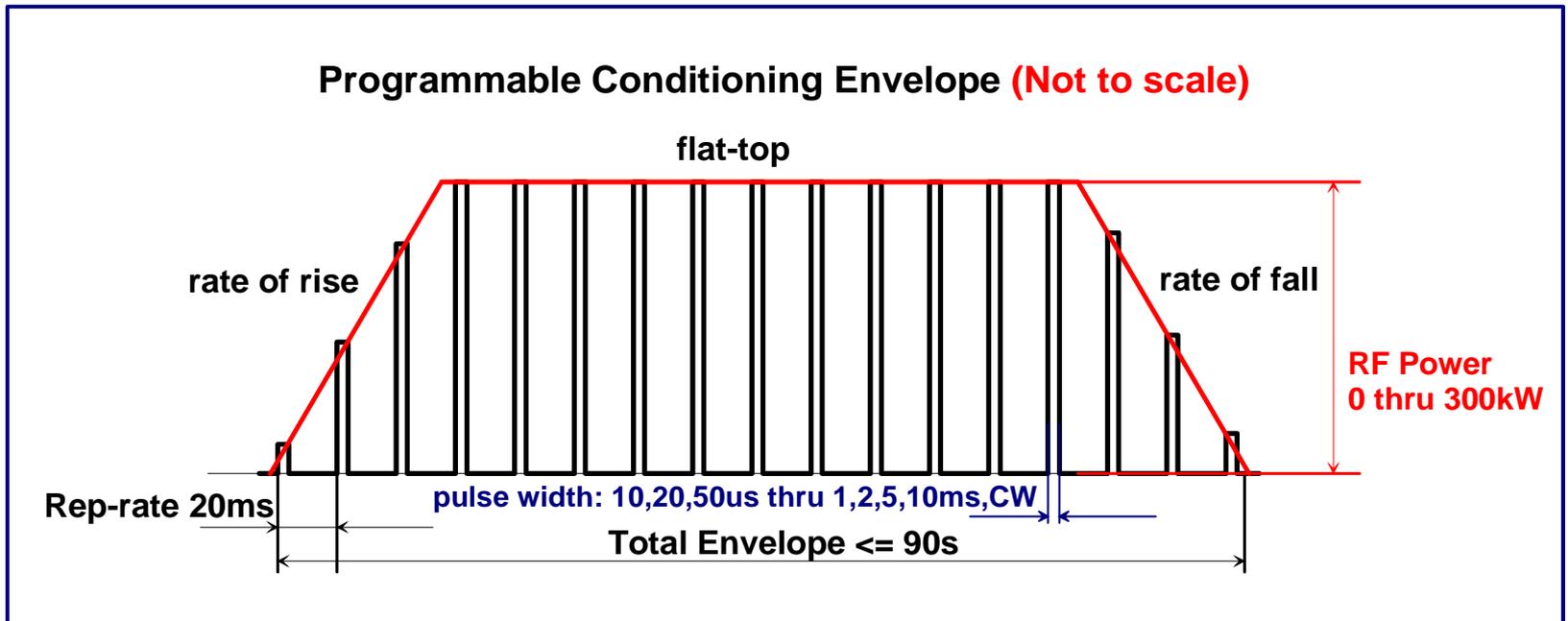
# LHC SC RF Conditioning

## ■ Requirements

- Initial conditioning of cavity field to 10 MV/m and 300kW CW power on the coupler for different coupling ratios
- The LHC SC cavities will need regular conditioning runs between machine fills to maintain the system performance.
- Concurrent operation **on all 16 cavities** to save time.
- Full remote control (no access to the LL electronics during run).
  - Automatic operation
  - Logging of power and vacuum data
  - Avoid special system re-configuration i.e. changing cables
- Highly reliable fail-safe vacuum loop and interlocks to avoid damage to the RF couplers.
- Pulsed and FM operation

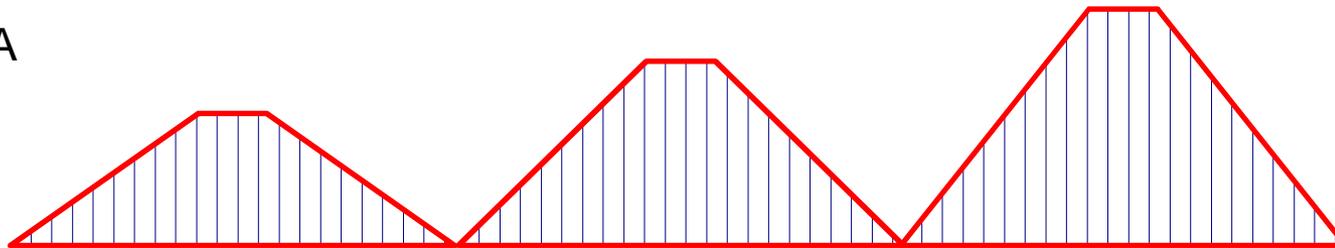
# Classic Method

- Pulsed FM modulated RF power is applied to the cavity in a controlled way with vacuum feedback
- Two loops
  - Fast vacuum feedback
  - Slow computer controlled loop to generate AM envelope and increase field and power as conditioning progresses



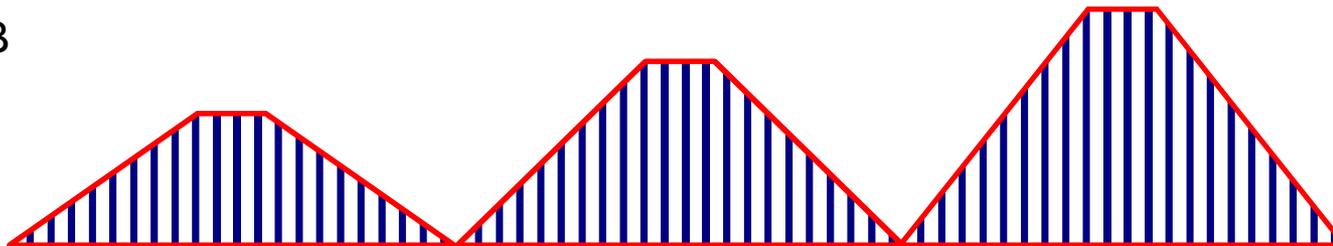
# Classic Method

A



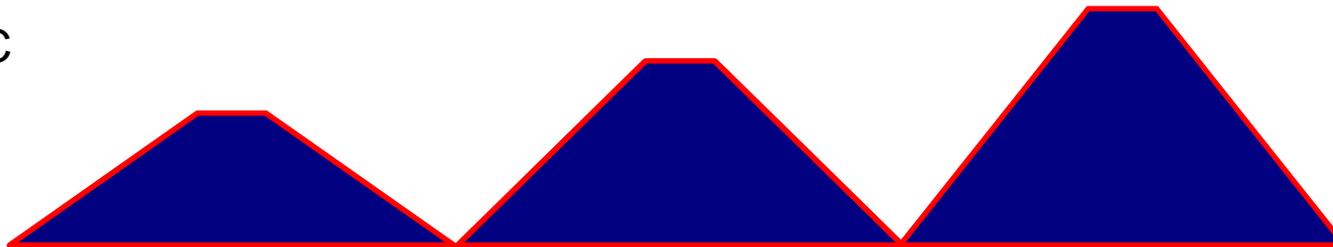
Increase Power using a fixed pulsewidth until Pmax is reached.

B



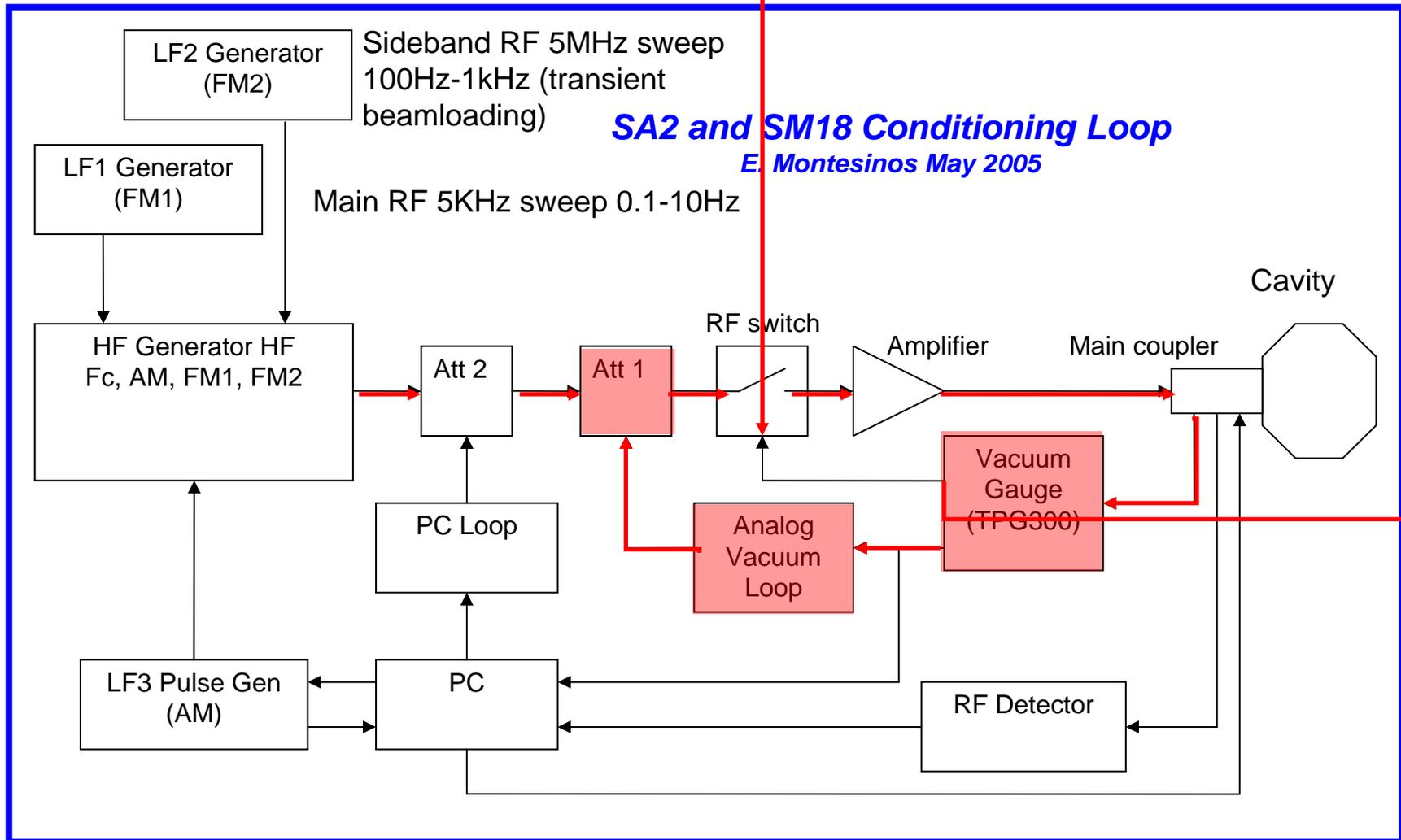
Increase Pulse width and proceed with the Power as above.

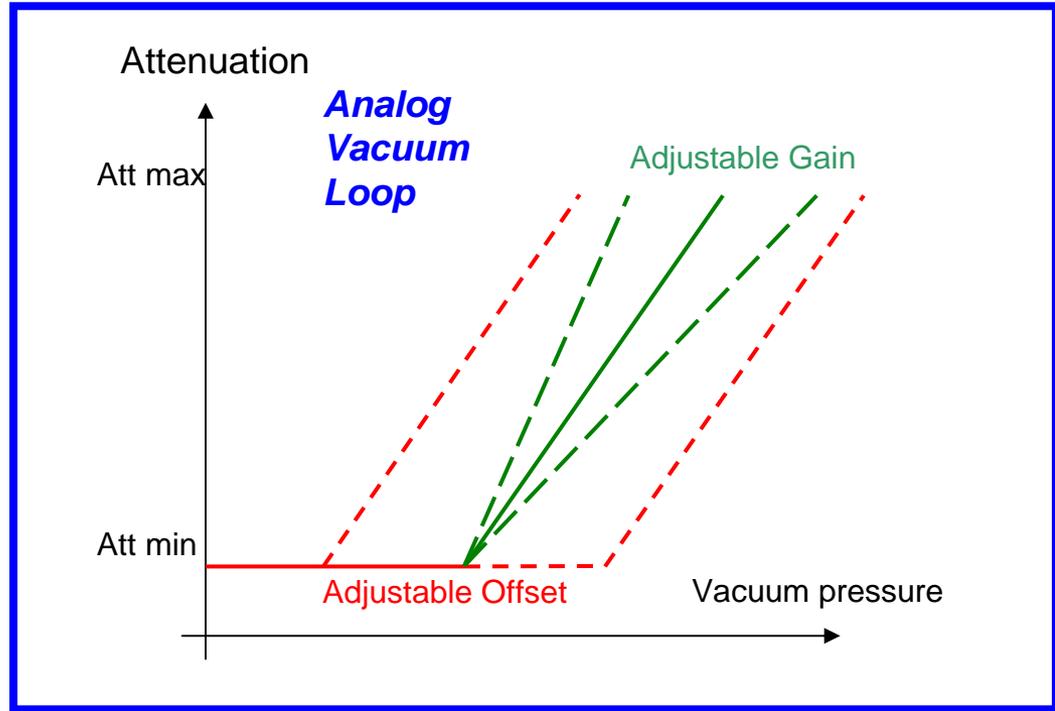
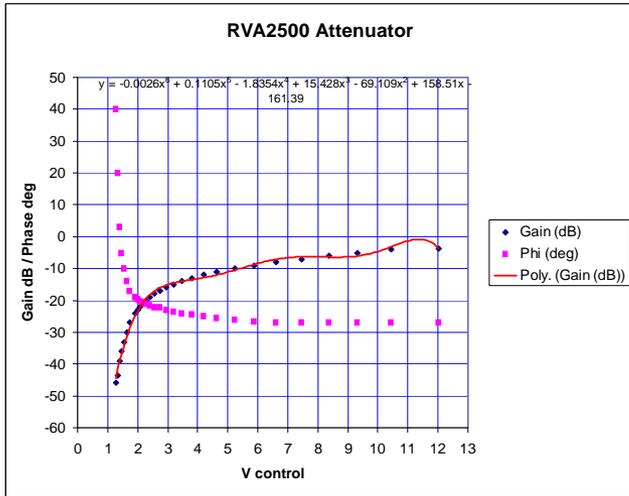
C



Finish with CW and proceed with the Power as above.

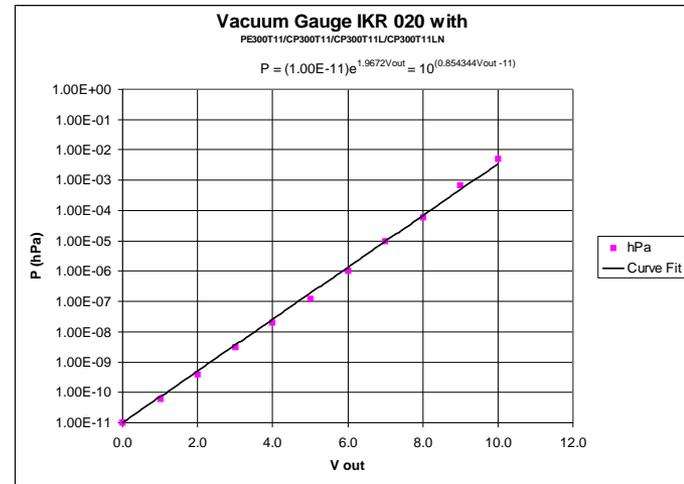
# Analog Conditioning System (until Dec. 2006)





## ■ Analog Vacuum Loop

- Manually adjusted loop
  - Offset
  - Gain
- Fail-safe passive attenuator
- Analog Vacuum gauge output



# LHC SC RF Conditioning

## ■ Motivation for a new Digital System

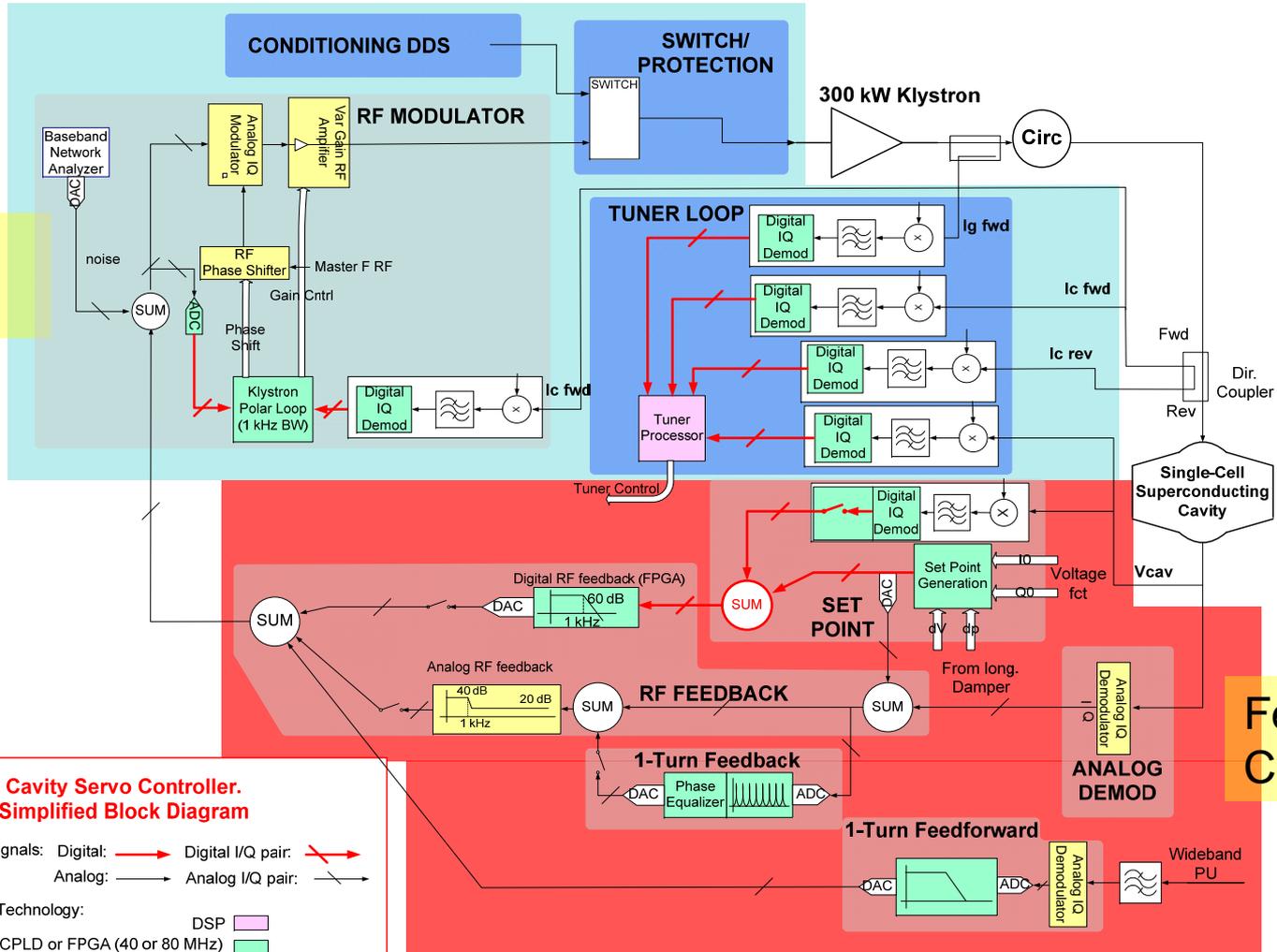
- The LHC SC conditioning system must be **integrated into each** cavity controller enabling remote operation through the VME interface.
- The use of off-the-shelf RF & LF generators is unpractical and too space demanding. (16 systems !)
- Embedded history and diagnostics
- Requirement to maintain tuning in pulsed mode

## ■ Implementation

- New solution resident in the cavity controller, uses the VME CPU, the Conditioning DDS, the “Switch & Protect” and the Tuner Loop Modules.
- Fail-safe vacuum loop operation cannot be implemented in an FPGA due to S.E.U. issues on Static RAM. A CPLD based on flash-ROM can be considered radiation tolerant.

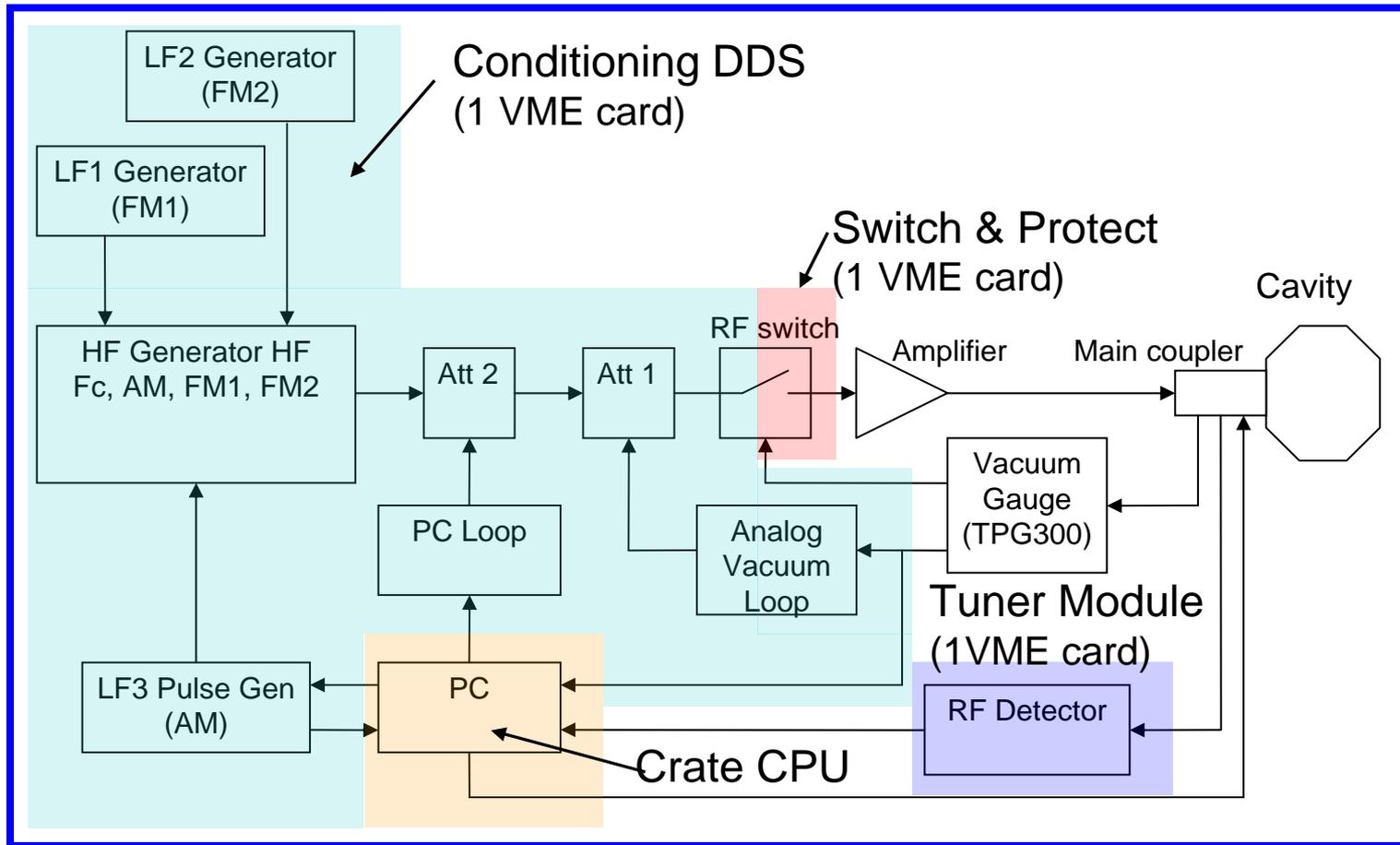
# Cavity Controller

Tuning  
Crate



Feedback  
Crate

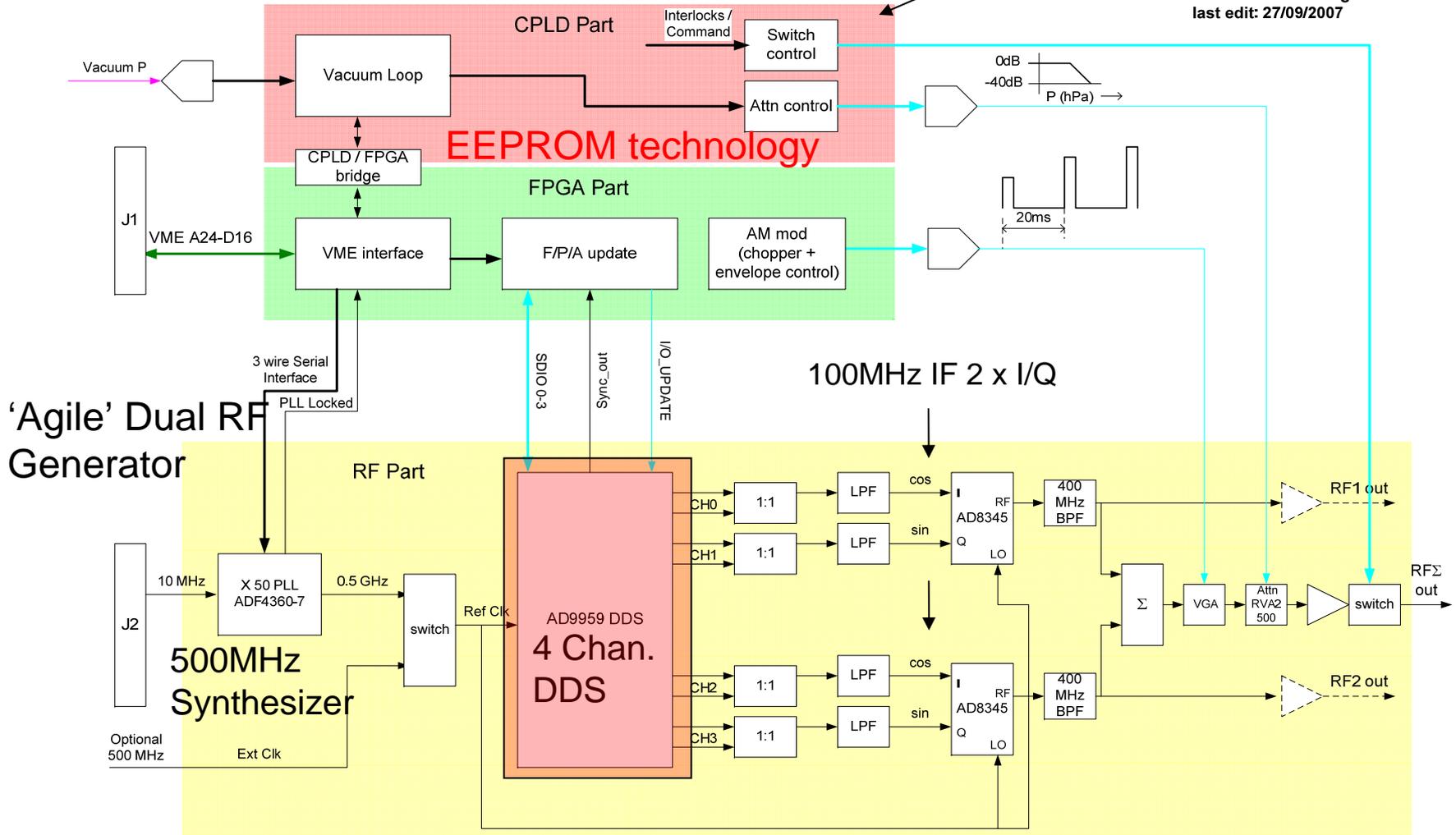
# New Digital System vs. Initial solution



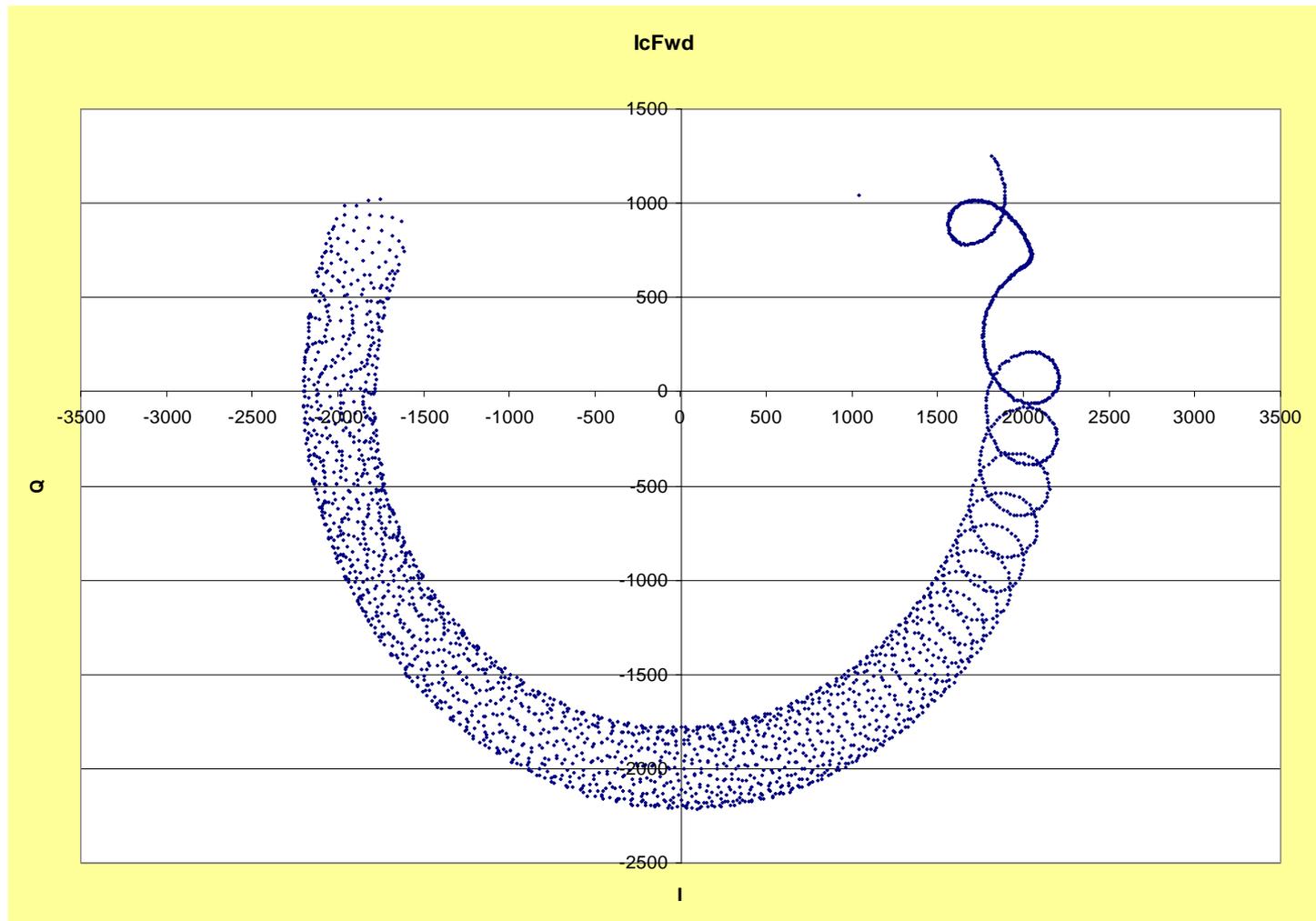
# Conditioning DDS Block diagram

Radiation tolerant  
fail-safe  
implementation

Dual DDS Module  
version: conditioning  
last edit: 27/09/2007



# Conditioning DDS – I/Q plot of Dual FM sweeps



Actual Data Obtained from Forward Current, I/Q memory in the Tuner loop module

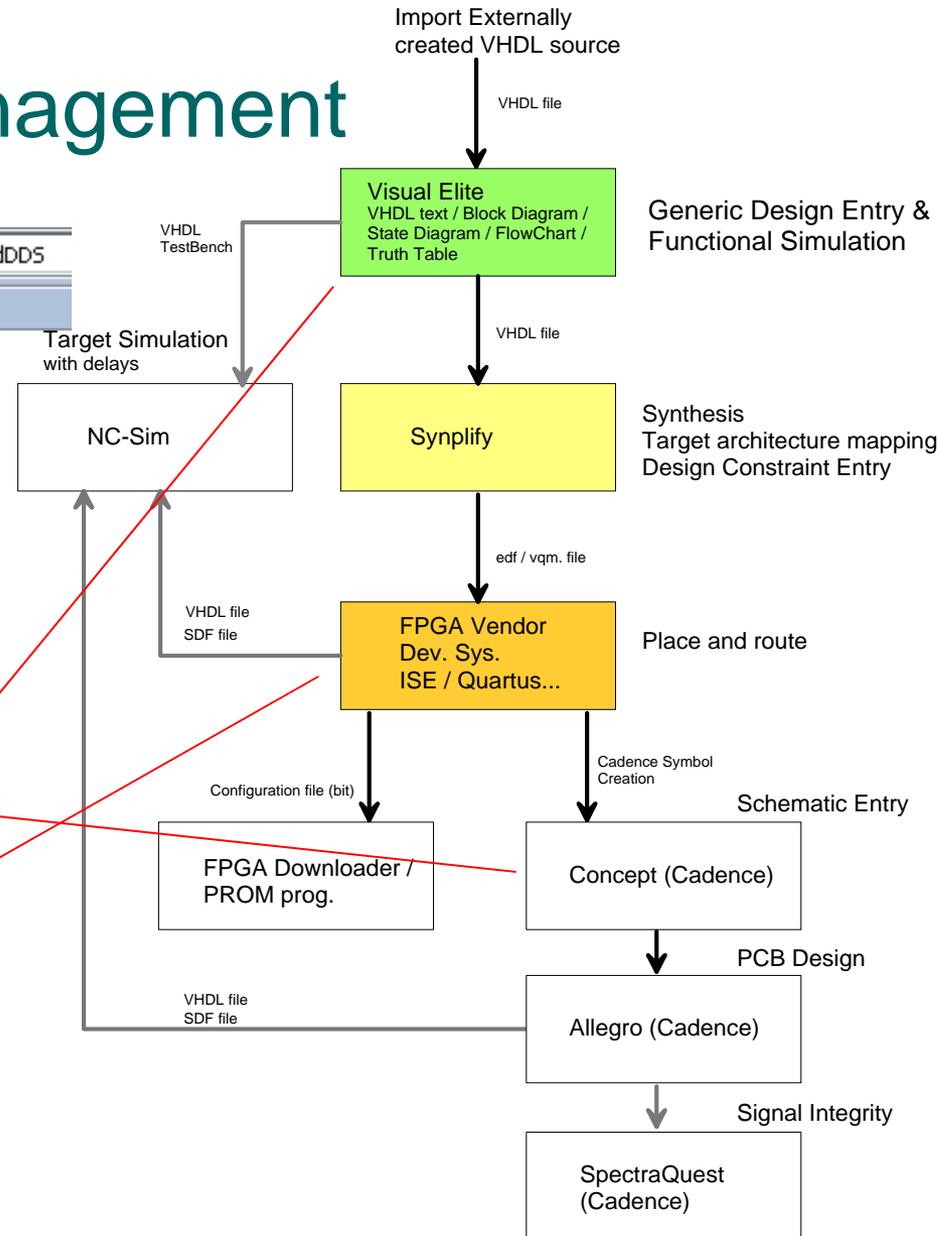
# Design Flow & Management

G:\Departments\AB\Groups\RF\Machines\LHC\LowLevel\Modules\QuadDDS

- + ClockGen
- + CommonCad
- + DCto100MHzDistr
- + Doc
- + FrevDistr
- + InjPulseGen
- + KlystronLoop
- + LHC\_1TFDBK
- + LLLoops
- + LLRFBP
- + OpticalLinkAna
- + PreDriver
- + **QuadDDS**
  - + Cadence
  - + Conditioning
  - + Lattice
  - + VCO 500MHz
  - + Visual
  - + Xilinx
- + RFfeedback
- + RFModulator

Cadence Reusable blocks

Design Repository



# FPGA Design Overview P & R

DDSFPGA Project Status			
<b>Project File:</b>	DDSFPGA.ise	<b>Current State:</b>	Programming File Generated
<b>Module Name:</b>	QuadDDSTop	• <b>Errors:</b>	No Errors
<b>Target Device:</b>	xc4vlx15-10ff668	• <b>Warnings:</b>	<a href="#">2 Warnings</a>
<b>Product Version:</b>	ISE 9.1.03i	• <b>Updated:</b>	Wed 17. Oct 10:17:20 2007

Occupation

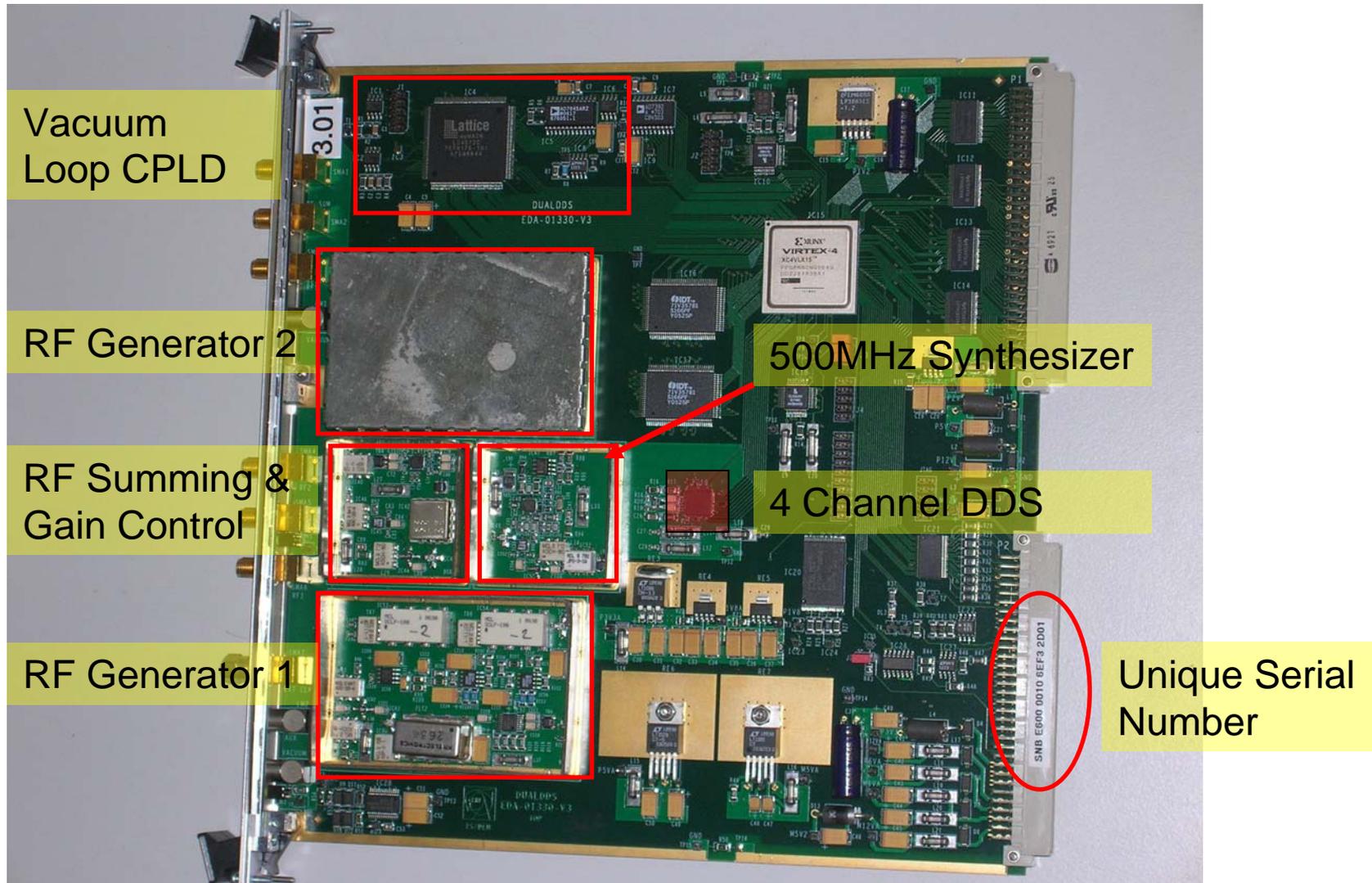
Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	1,673	12,288	13%	
Number of 4 input LUTs	2,320	12,288	18%	
<b>Logic Distribution</b>				
Number of occupied Slices	1,940	6,144	31%	
Number of Slices containing only related logic	1,940	1,940	100%	
Number of Slices containing unrelated logic	0	1,940	0%	
<b>Total Number of 4 input LUTs</b>	<b>2,705</b>	<b>12,288</b>	<b>22%</b>	
Number used as logic	2,320			
Number used as a route-thru	129			
Number used for Dual Port RAMs	256			
Number of bonded <a href="#">IOBs</a>	262	320	81%	
Number of BUFG/BUFGCTRLs	3	32	9%	
Number used as BUFGs	3			
Number used as BUFGCTRLs	0			
Number of FIFO16/RAMB16s	8	48	16%	
Number used as FIFO16s	0			
Number used as RAMB16s	8			
<b>Total equivalent gate count for design</b>	<b>572,357</b>			
Additional JTAG gate count for IOBs	12,576			

Overall Gate-count

Ready to run

Performance Summary			
<b>Final Timing Score:</b>	0	<b>Pinout Data:</b>	<a href="#">Pinout Report</a>
<b>Routing Results:</b>	<a href="#">All Signals Completely Routed</a>	<b>Clock Data:</b>	<a href="#">Clock Report</a>
<b>Timing Constraints:</b>	<a href="#">All Constraints Met</a>		

# The Conditioning DDS Module



# The Cavity Controller Tuning Crate

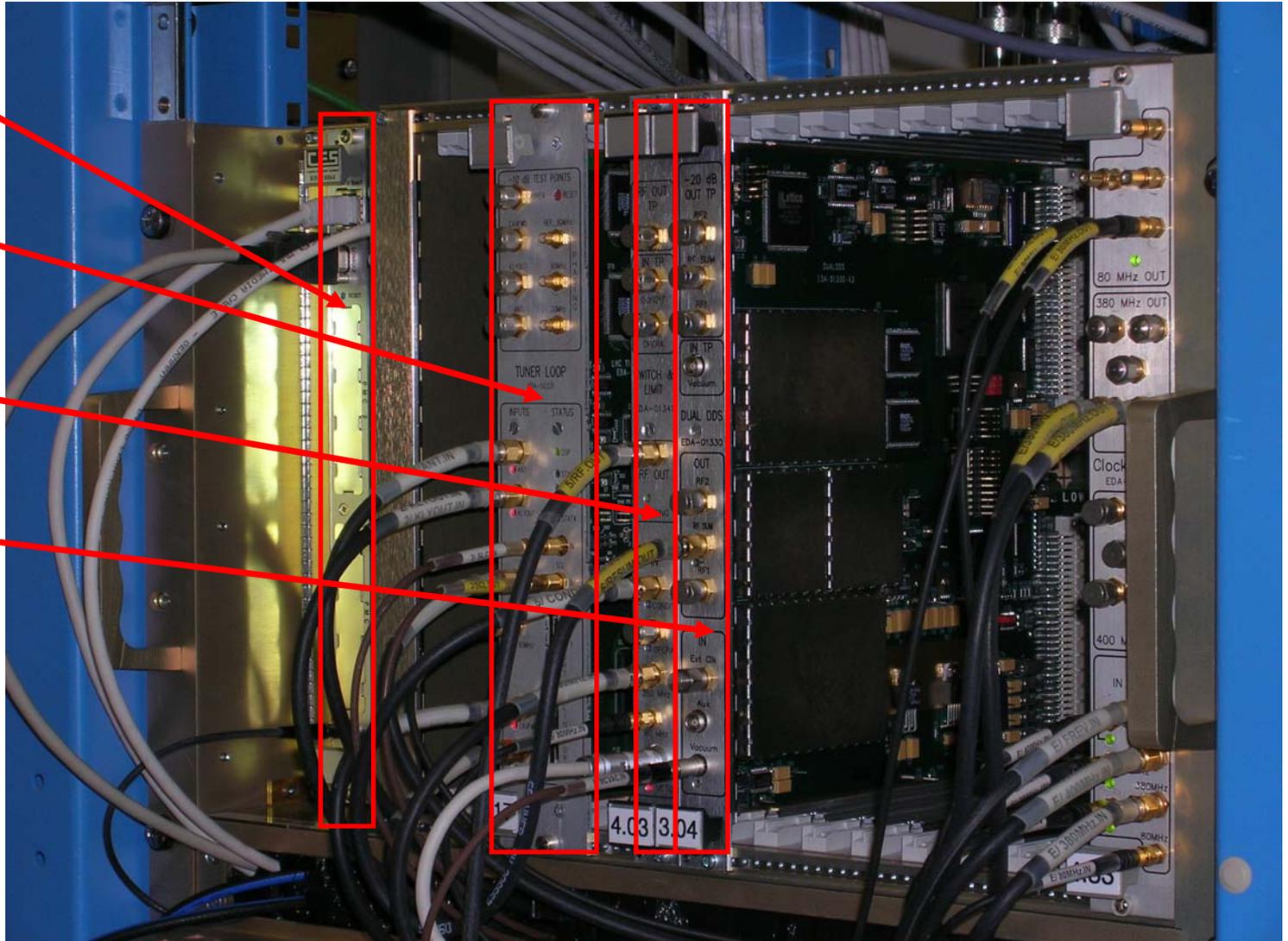
(Installed in 8 out of 16 cavities, Oct. 07)

VME CPU

Tuner Loop

Switch &  
Protect

Conditioning  
DDS



# Software architecture

## ■ Based on the CERN Standard Architecture

(see reference: ICALEPCS-10)

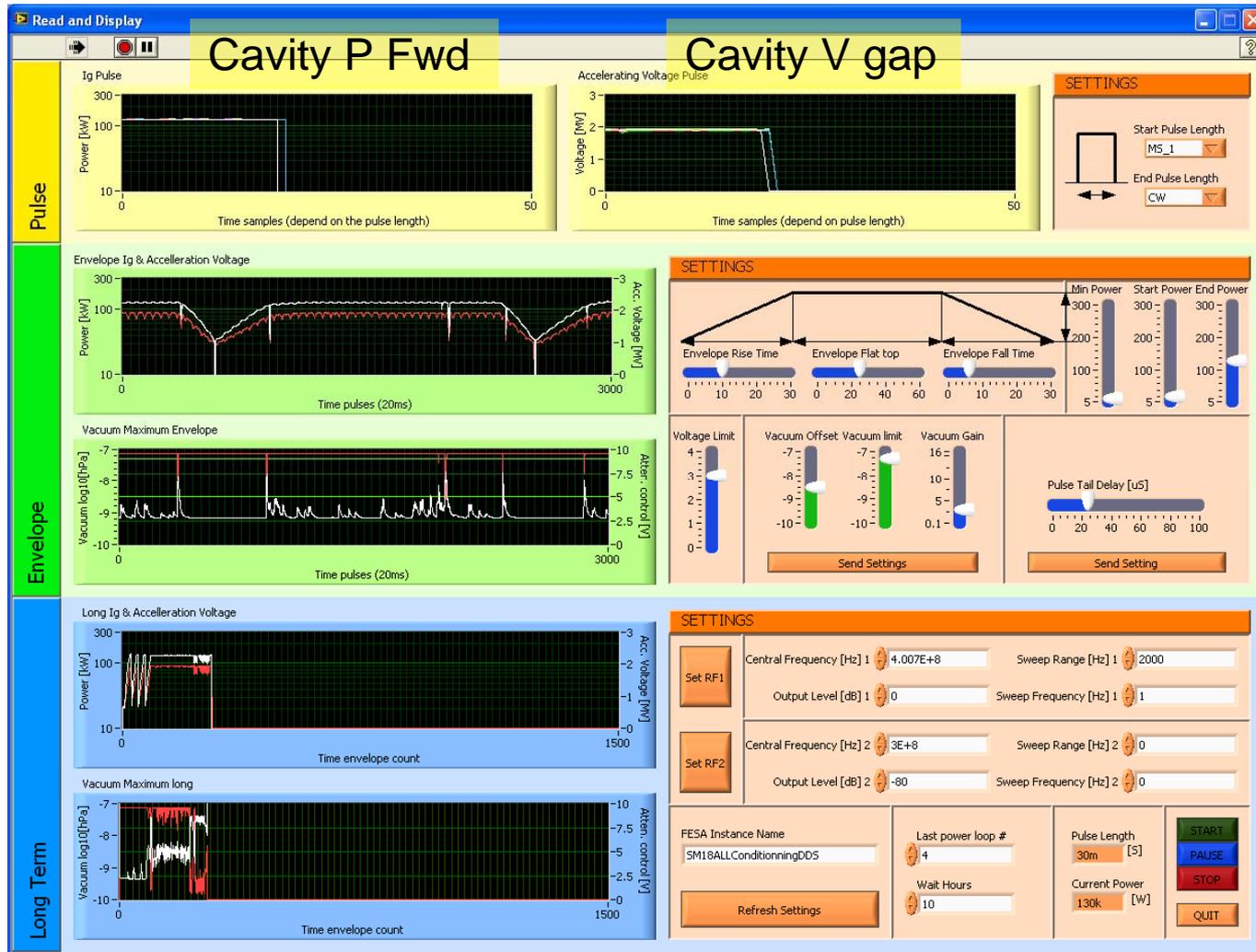
- Driver
  - Front-End Software Architecture (FESA)
  - Controls MiddleWare (CMW)
  - Application layer JAVA...
- ## ■ The current conditioning application
- Uses an additional FESA wrapper to interface with LabView
  - GUI made with LabView.

# Conditioning - Real-time operation

- The conditioning DDS Module generates IRQs and issues crate-wide observation triggers at a 50Hz rate
  - The IRQs trigger the FESA conditioning class that acquires cavity power, gap voltage, vacuum, vacuum gain and status from the cond. DDS and the Tuner Loop modules.
  - The conditioning class regulates the RF power using the Tuner Loop power acquisition ( $I^2+Q^2$  of Cavity Fwd channel).
  - The conditioning class regulates the cavity gap voltage using the Tuner Loop voltage acquisition ( $I^2+Q^2$  of Antenna channel).
  - Back-off the demanded power if the vacuum gain issued by vacuum loop exceeds the working point.
  - The conditioning DDS module disables both the IRQ source and the RF drive if 8 successive IRQs were not serviced.

Whichever  
is first

# LHC SC RF Conditioning - LabView GUI



Controls

Pulse

Envelope & Power

Vacuum Loop

Dual FM Generator

Global

# Conclusions and Outlook

- SM18 first tests successful
- Close collaboration between power, LL RF, digital design and software specialists with clear definition of
  - Mode of operation
  - Interfaces between analog, RF hardware & Software
- The initial prototype worked with very few changes and allowed an immediate launch of series production
- 25 boards fabricated and tested
  - The entire series did not require any reworking and passed all validation tests
- Currently installed 8 of 16 systems in UX45 Faraday cages
  - Presently used for Klystron power tests
- Ready for operation in November 2007

# References

## ■ ICALEPCS-10 (2005)

- “Control Of The Low Level RF System Of The Large Hadron Collider”, P1\_028

A. Butterworth, J. Molendijk, R. Sorokoletov, F. Weierud (CERN, Geneva)

## ■ LLRF05

- “Complex Digital Design For The LHC Low Level RF”, J.C. Molendijk (CERN Geneva)

## ■ EPAC06

- “Digital Design of the LHC Low Level RF – the Tuning System for the Superconducting Cavities”, TUPCH196

John C. Molendijk, Philippe Baudrenghien, Andrew Butterworth, Edmond Ciapala, Ragnar Olsen, Frode Weierud (CERN, Geneva), Roman Sorokoletov (JINR, Dubna, Moscow Region).

## ■ SRF2007

- “Construction and Processing of the Variable RF Power Couplers for the LHC Superconducting Cavities”, E. Montesinos (CERN, Geneva).



Thank you for your attention.

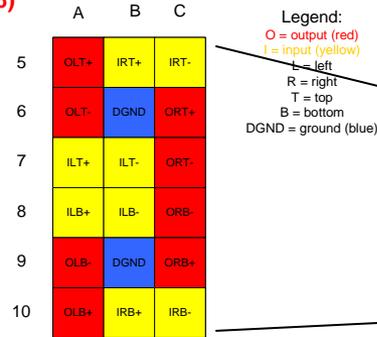
# LHC RF System

- 16x 400MHz Superconducting Cavities (8 per ring)
- 1x 300kW klystron per cavity
- Sophisticated Low Level RF Loops for cavity control, beam control and synchronization.

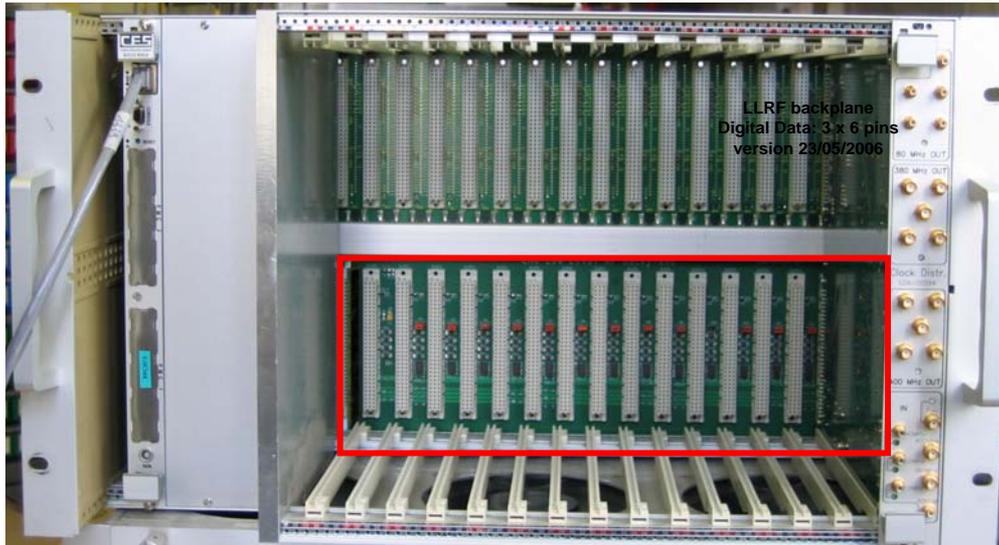


# LHC LL RF Backplane

Digital data  
(3x6)

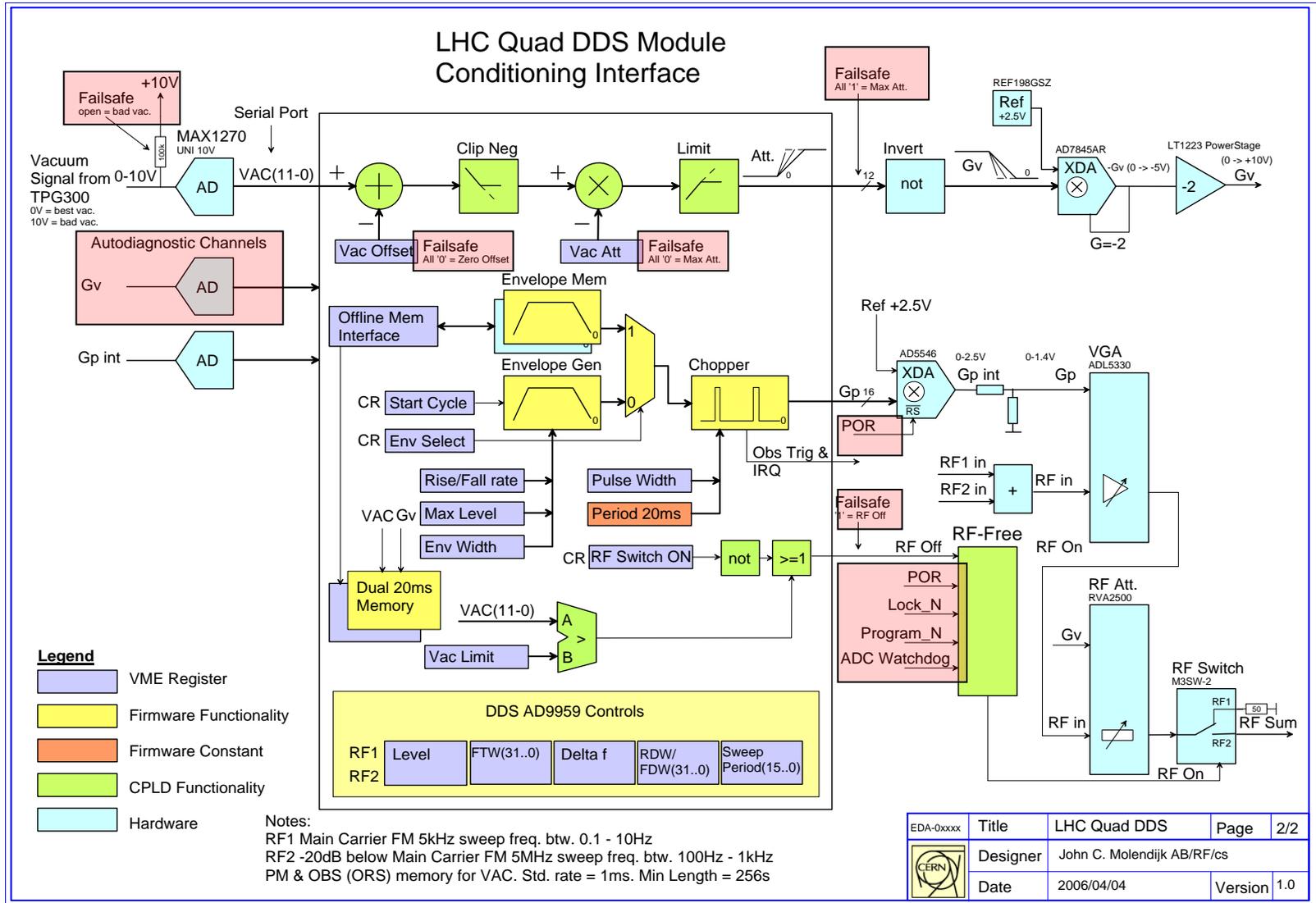


Digital data: 4 serial inputs and 4 serial outputs per connector. Inputs/outputs routed to neighboring cards.



		A	B	C	
1	<b>Timings (12x)</b>	Cycle Start*	● ● ●	BpTB1*	AnalyzeTrig*
		Beam In*	● ● ●	BpTB2*	Post-mortem Trig*
		BpTA3* / Beam Out*	● ● ●	BpTB3*	Observation Trig*
		BpTA4*	● ● ●	BpTB4*	Cold reset*
4					
5					
8	<b>Digital data (3x6)</b>				See page 2
10					
13	<b>Intlk/Alarm (3x) FG</b>	Inj Enable	● ● ●	ConfigDone	
		SDin	● ● ●	DGND, SDout	
21	<b>Clocks (Differential ECL) + Module Address (MA3-0)</b>	spare	● ● ●	spare	
		40 MHz-	● ● ●	40 MHz+	
		spare	● ● ●	spare	
		20 MHz-	● ● ●	20 MHz+	
		MA0	● ● ●	MA1	
		10 MHz-	● ● ●	10 MHz+	8 x DGND
		MA2	● ● ●	MA3	
		Frev-	● ● ●	Frev+	
26	<b>Jtag</b>	TDI	● ● ●	DGND, TDO	
		TCK	● ● ●	!ENA, TMS	
32	<b>Extra Digital V</b>		● ● ●	+3.3 V	<b>Switched Mode Power Supply</b>
			● ● ●	DGND	
32	<b>Analog Power Supply + AGND (3 pins each)</b>	spare	● ● ●	AGND	<b>Linear Power Supply</b>
			● ● ●	Module Serial Number Bus	
			● ● ●	+12 V	
			● ● ●	+6 V	
			● ● ●	-6 V	
			● ● ●	-12 V	

# Conditioning DDS Interface



# Single Event Upset

## Soft Errors – Current Product Families

### ORCA, XPGA, XPLD

- Current Product Families based on 0.16 – 0.18um technology

Product	Supply Voltage	Technology	Neutron SER Rate (FIT/Mbit) (SEU Xsect)	Alpha SER Rate (FIT/Mbit)	Logic SER Rate (FIT)	Total SER Rate (FIT/Mbit)
OR4E	1.5V	COM2	<150 <9.1E-15	<450	N/A	<600
FPSC	1.5V	COM2	<150 <9.1E-15	<450	N/A	<600
XPLD	1.8V	EE9	<400 <3.7E-14	<1200	<10	<1600
XPGA	1.8V	EE9	<450 <3.9E-14	TBD	<10	TBD
CPLD	1.8V	EE9	N/A	N/A	<10	<10

\* - Actual data shown from Neutron beam testing at Los Alamos, and Alpha Source testing at LSC. No indication of Single Event Latch-up was detected during testing.

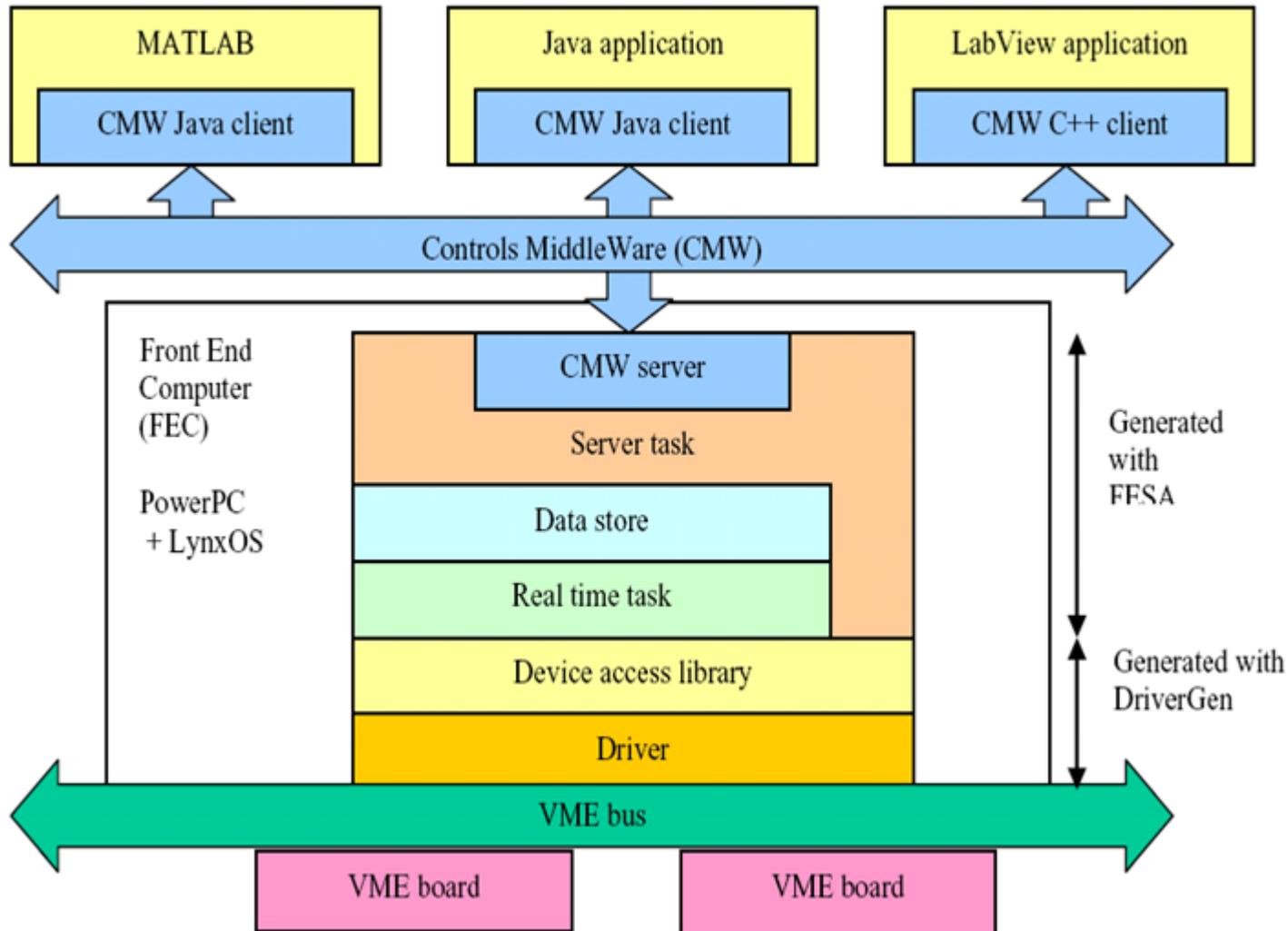
Revision 1, Apr 24, 2004

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Page 1

  
Lattice  
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Corporation  
Bringing the Best Together

# CERN Standard Architecture



# LHC SC RF Conditioning – Tuner lock-in

Approaching Resonance

The software interface displays real-time data for the LHC SC RF Conditioning system. It includes the following components:

- Pulse Section:**
  - Cavity P Fwd:** Plot of Power [kW] vs Time samples (depend on the pulse length).
  - Cavity V gap:** Plot of Accelerating Voltage Pulse [MV] vs Time samples (depend on pulse length).
  - SETTINGS:** Start Pulse Length (MS\_1), End Pulse Length (CW).
- Envelope Section:**
  - Envelope Ig & Acceleration Voltage:** Plot of Power [kW] and Acc. Voltage [MV] vs Time pulses (20ms).
  - Vacuum Maximum Envelope:** Plot of Vacuum log<sub>10</sub>[hPa] and Atten. control [V] vs Time pulses (20ms).
  - SETTINGS:** Envelope Rise Time, Envelope Flat top, Envelope Fall Time, Min Power, Start Power, End Power, Voltage Limit, Vacuum Offset, Vacuum limit, Vacuum Gain, Pulse Tail Delay [μs].
- Long Term Section:**
  - Long Ig & Acceleration Voltage:** Plot of Power [kW] and Acc. Voltage [MV] vs Time envelope count.
  - Vacuum Maximum long:** Plot of Vacuum log<sub>10</sub>[hPa] and Atten. control [V] vs Time envelope count.
  - SETTINGS:** Set RF1 (Central Frequency [Hz] 1: 4.0071E+8, Sweep Range [Hz] 1: 5000, Output Level [dB] 1: 0, Sweep Frequency [Hz] 1: 1), Set RF2 (Central Frequency [Hz] 2: 3E+8, Sweep Range [Hz] 2: 0, Output Level [dB] 2: -80, Sweep Frequency [Hz] 2: 0).
- Global SETTINGS:**
  - FESA Instance Name: SM18ALLConditioningDD5
  - Last power loop #: 4
  - Wait Hours: 10
  - Pulse Length: 30m [S]
  - Current Power: 150k [W]
  - Buttons: START, PAUSE, STOP, QUIT, Refresh Settings.