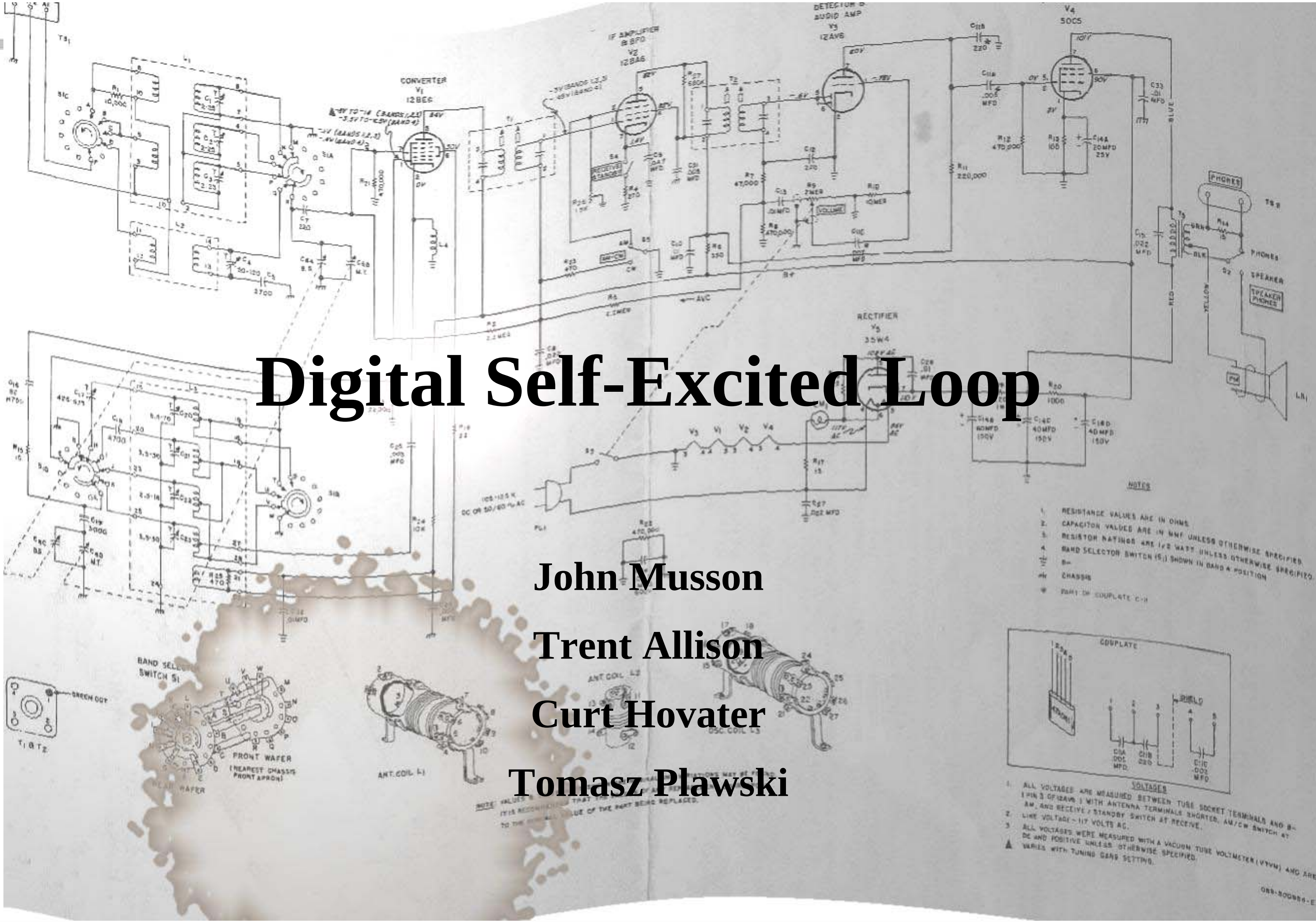


Digital Self-Excited Loop

John Musson

Trent Allison

Curt Hovater

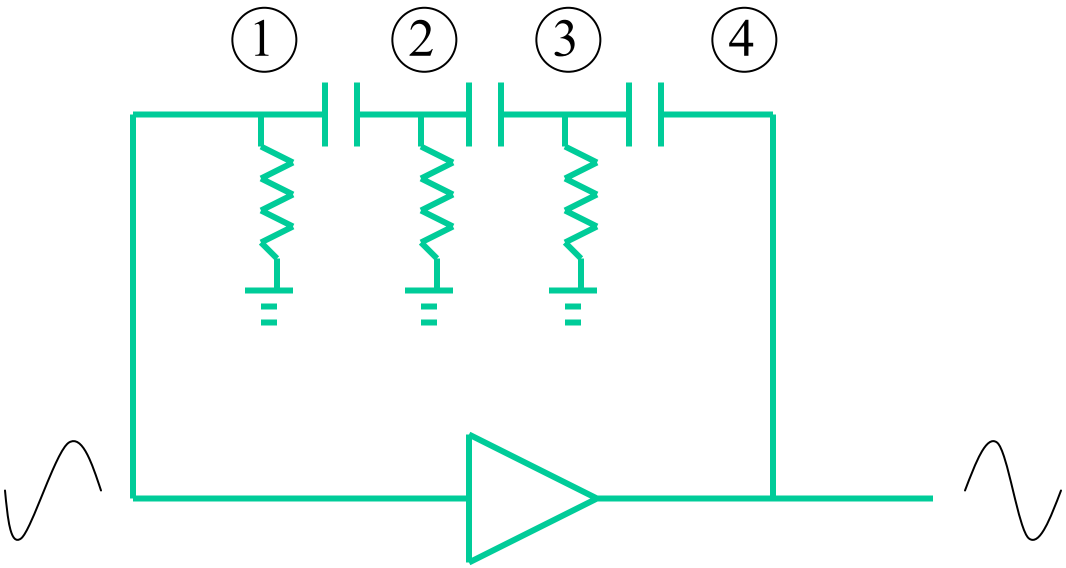
Tomasz Plawski

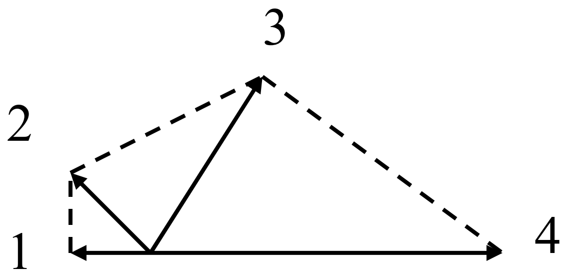
Oscillator Basics

FDN w/ 180-degree phase shift

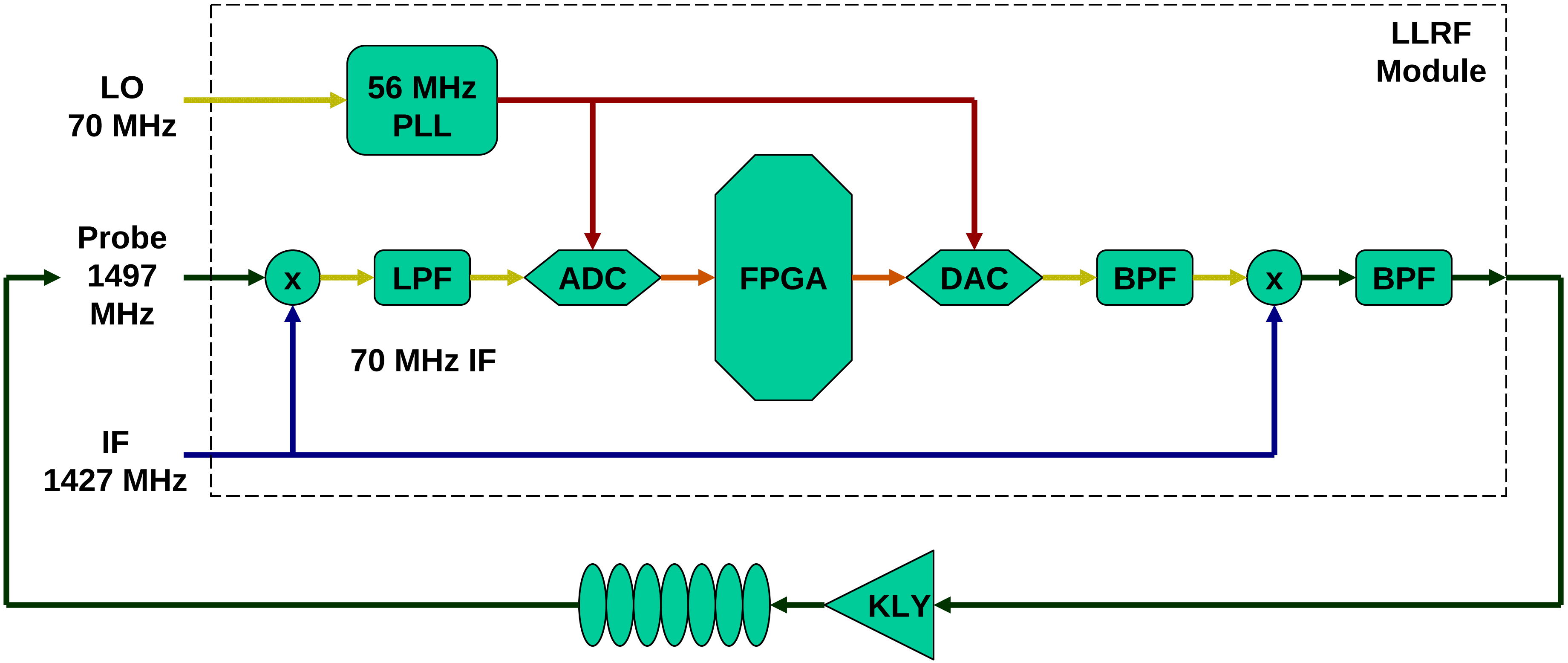
Gain > 1 at desired frequency

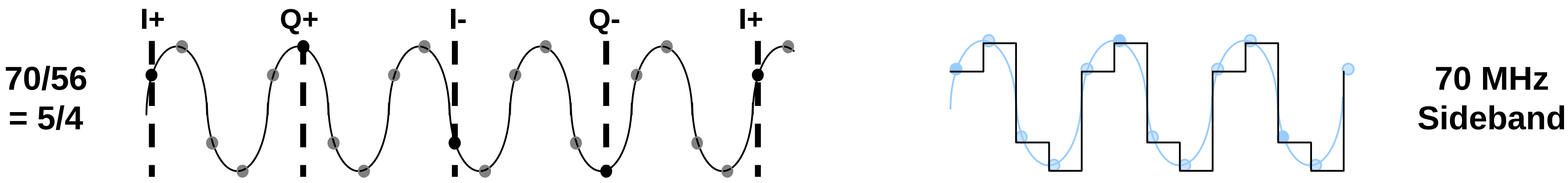
Amplitude stabilization…non-linear element





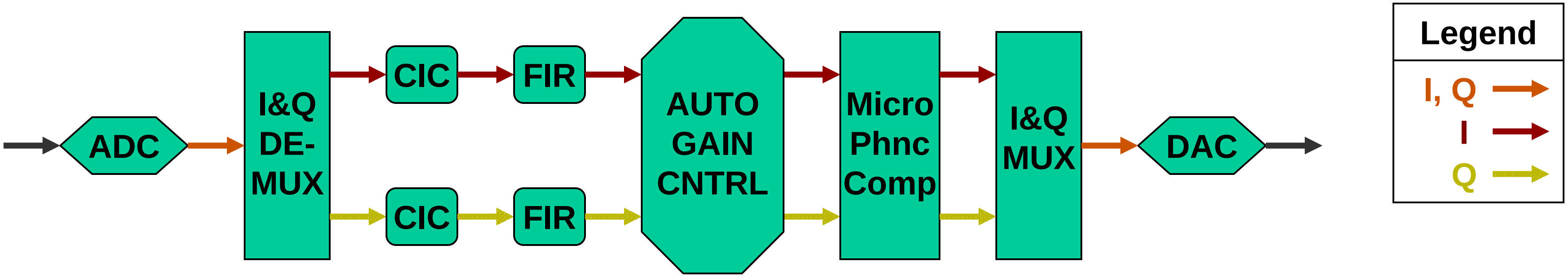
Digital SEL Implementation



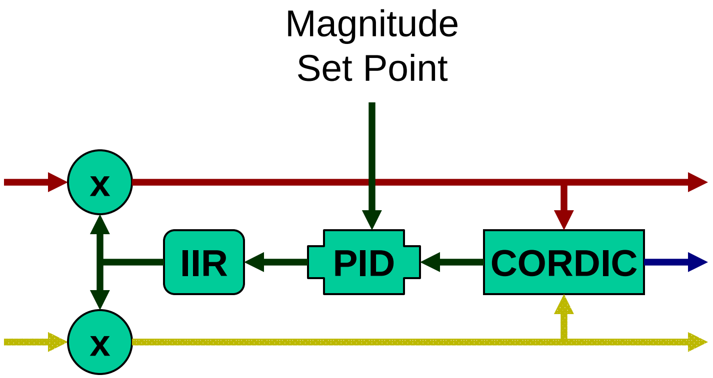


First SEL Block Diagram

AGC SEL



(Output) Automatic Gain Control*



"*Resonance-independent"

MO is implicit…56MHz ADC/DAC clock

I & Q must be allowed to tumble (AC)

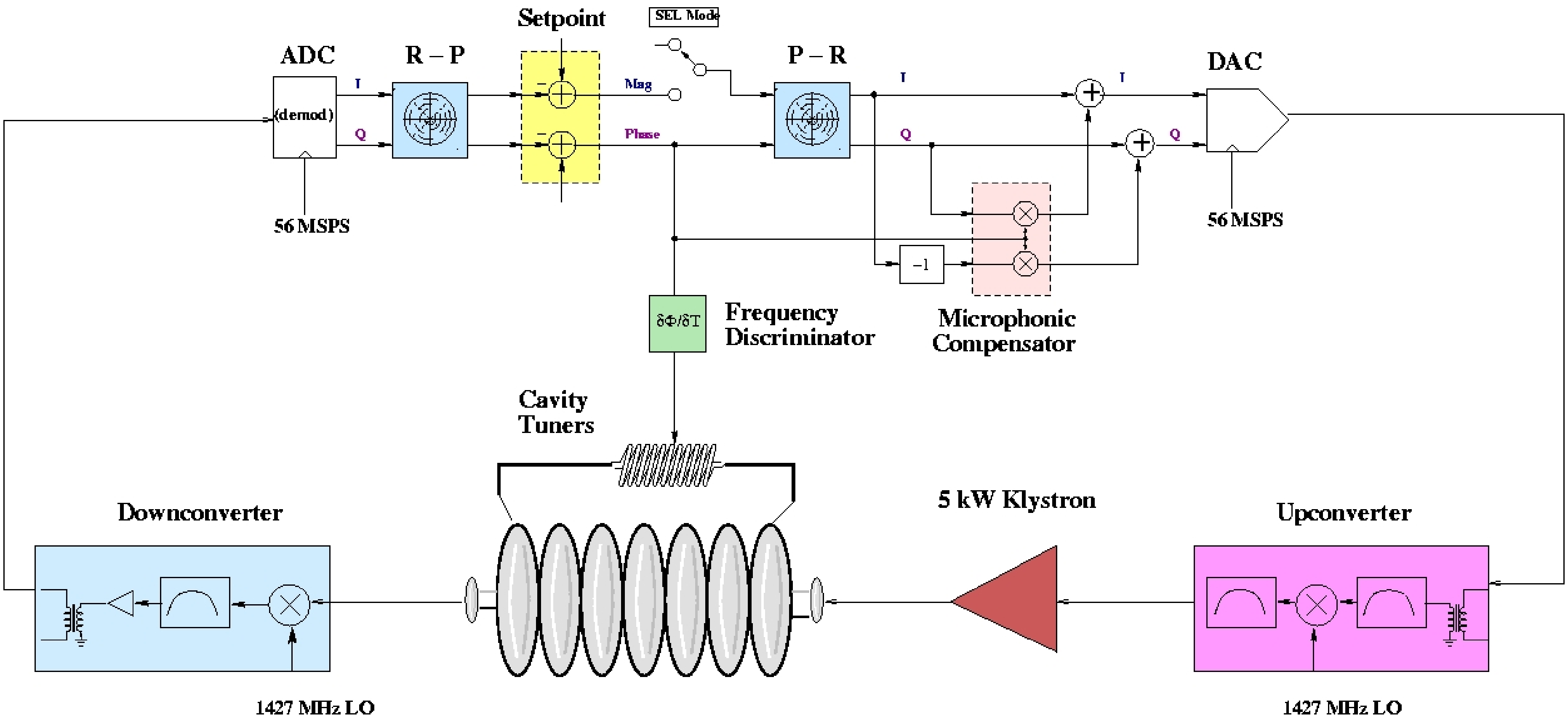
IIR Pole was necessary…..too slow

AGC was implemented in both directions:

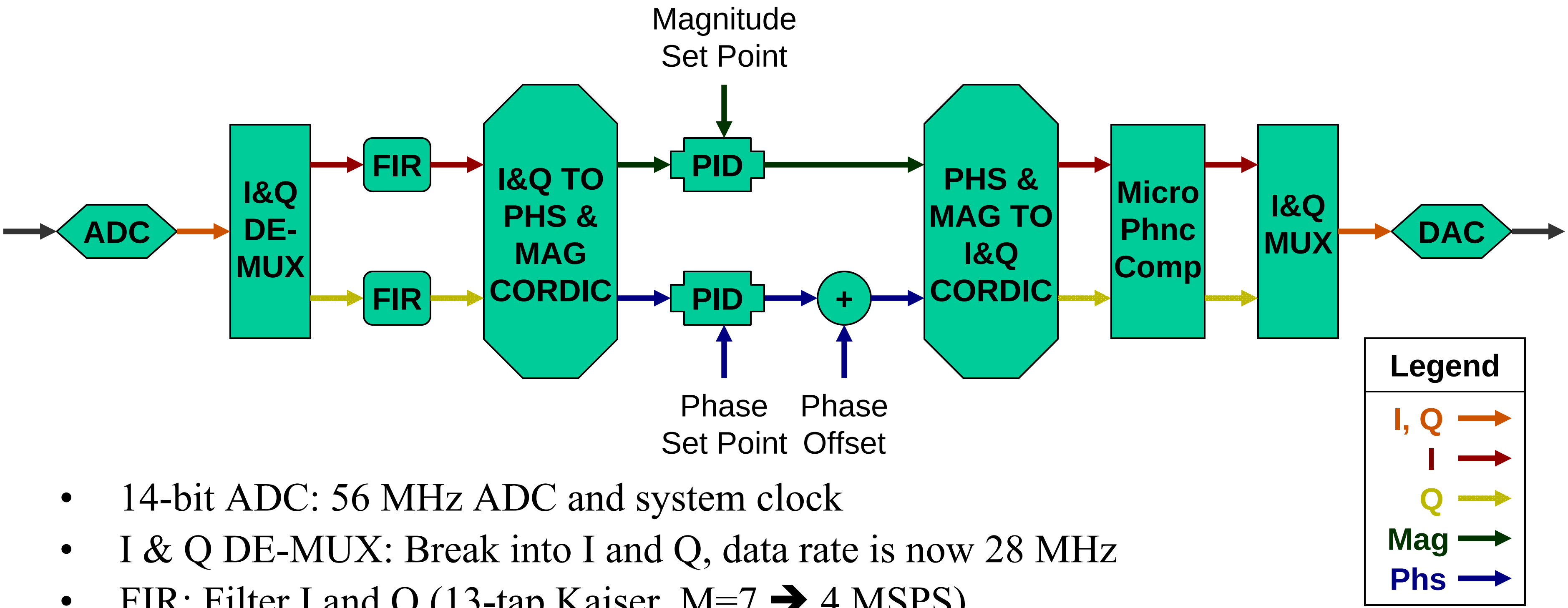
Output regulation

Input regulation

Polar Conversion Form



Present SEL Block Diagram… Detail



- 14-bit ADC: 56 MHz ADC and system clock
- I & Q DE-MUX: Break into I and Q, data rate is now 28 MHz
- FIR: Filter I and Q (13-tap Kaiser, M=7 ➔ 4 MSPS)
- CORDIC: Cartesian to Polar coordinate transformation, 16-bit
- PID: Phase and magnitude control
- Adder: Static phase shift
- CORDIC: Polar to Cartesian coordinate transformation
- Microphonics Compensation: I’ = I + (Q * Phserr), Q’ = Q - (I * Phserr)
- I & Q MUX: Combine I and Q to reconstruct signal at 56 MHz

FPGA Resources:
11.9k LE
18 9-bit DSP Blocks

CORDIC Digression…..

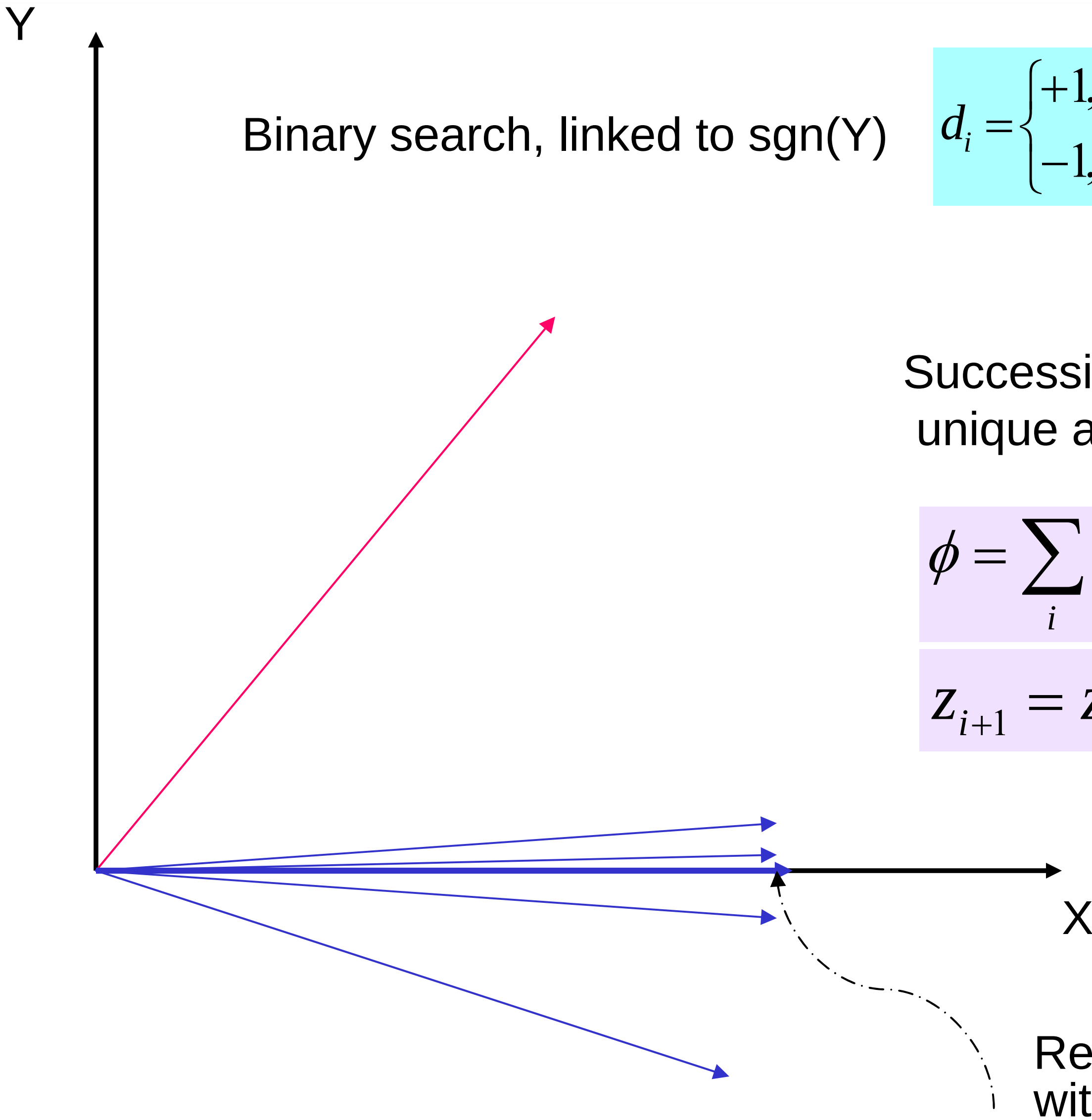
- Exploits the similarity between 45^o, 22.5^o, 11.125^o, etc. and Arctan of 0.5, 0.25, 0.125, etc.
- Multiplies are reduced to shift-and-add operations

Angle	Tan ( )	Nearest 2^{-N}	Atan ( )
45	1.0	1	45
22.5	0.414	0.5	26.6
11.25	0.199	0.25	14.04
5.625	0.095	0.125	7.13
2.8125	0.049	0.0625	3.58
1.406125	0.0246	0.03125	1.79
0.703125	0.0123	0.01563	0.90

$$[x', y'] = [x, y] \cdot \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}$$

$$x_{i+1} = K_i \left[x_i - y_i \cdot d_i \cdot 2^{-i} \right]$$
$$y_{i+1} = K_i \left[y_i + x_i \cdot d_i \cdot 2^{-i} \right]$$

Functionally.....



Binary search, linked to sgn(Y)

$$d_i = \begin{cases} +1, & if\ y_i < 0 \\ -1, & if\ y_i \geq 0 \end{cases}$$

Successively add angles to produce unique angle vector

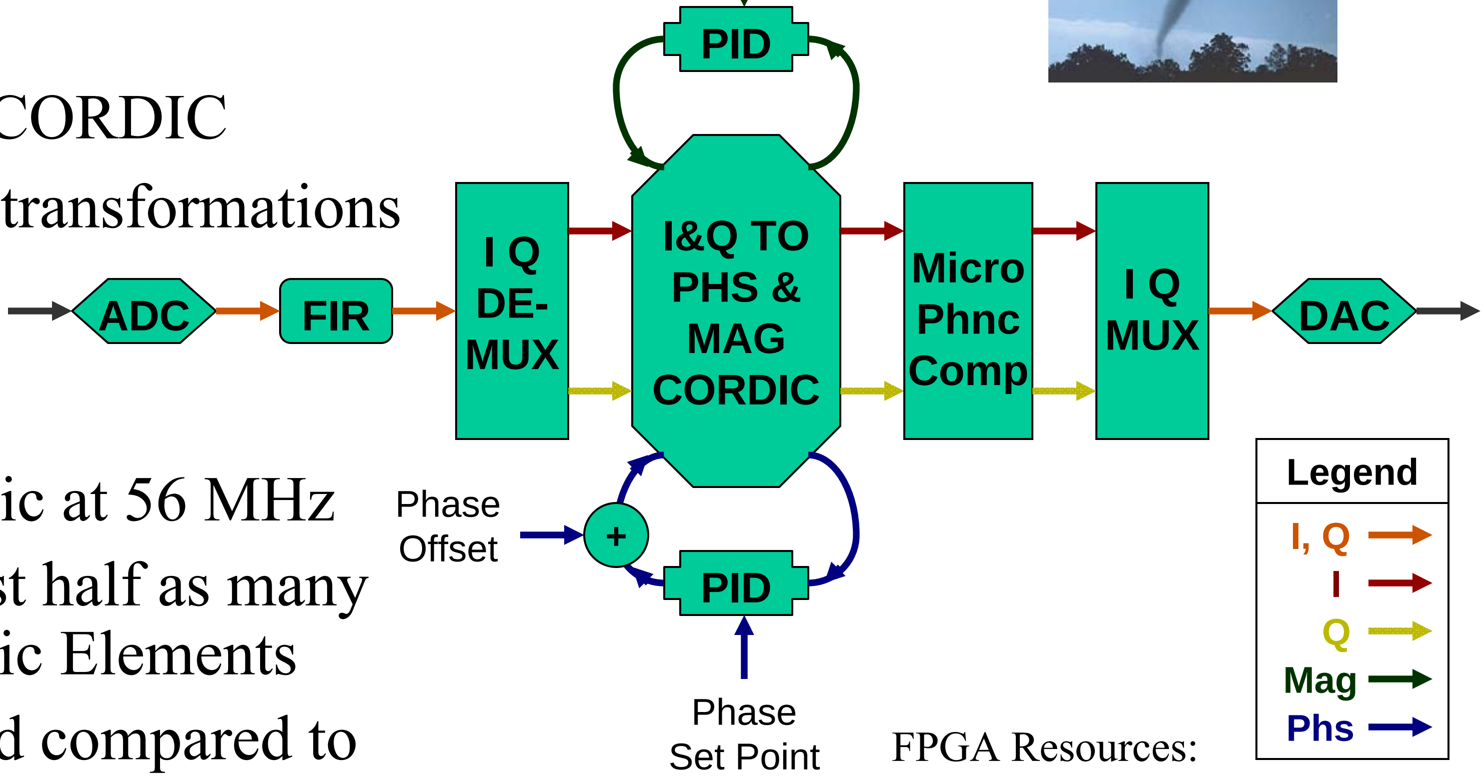
$$\phi = \sum_i d_i \cdot \arctan(2^{-i})$$

$$z_{i+1} = z_i - d_i \cdot \arctan(2^{-i})$$

Resultant lies on X (real) axis with a residual gain of 1.6

SEL Firmware Optimization

- Reduce to one interleaved FIR filter
- Interleave CORDIC coordinate transformations

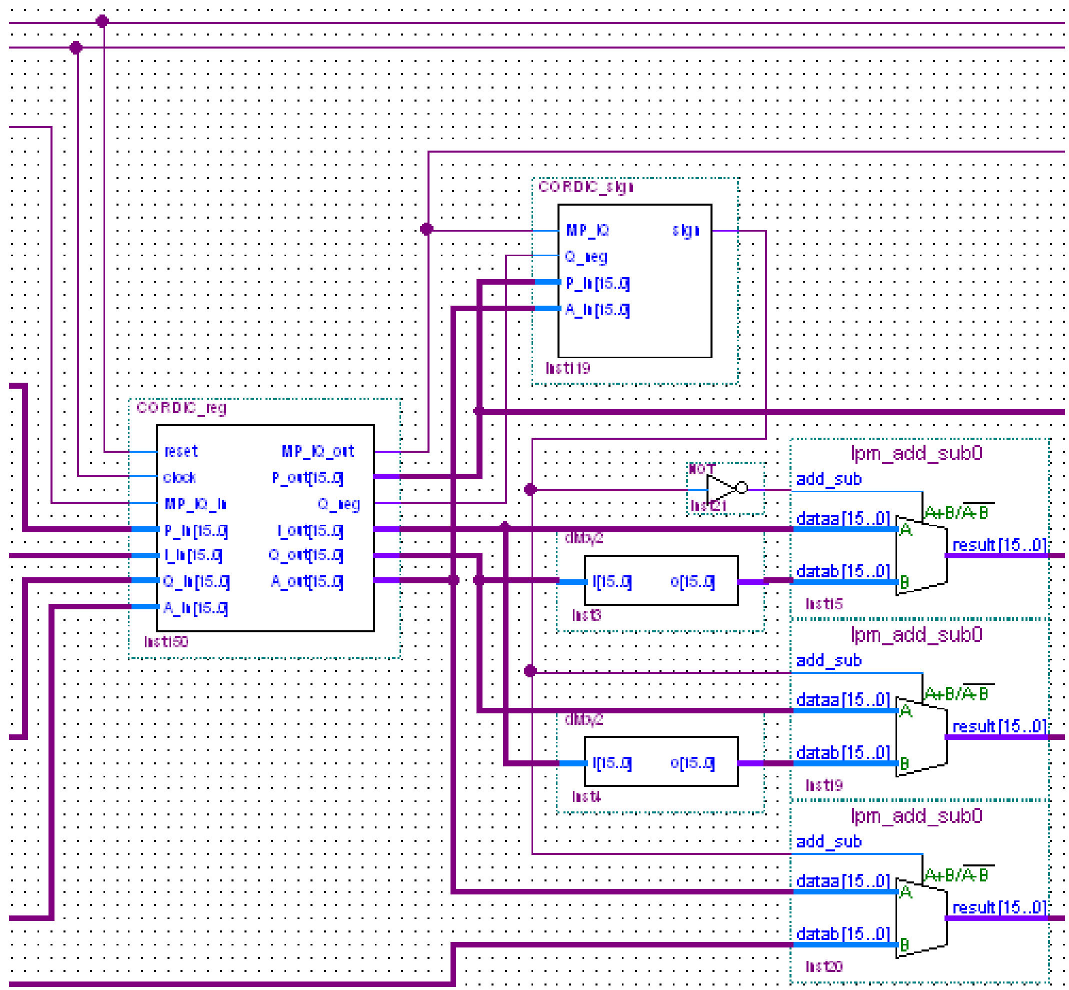


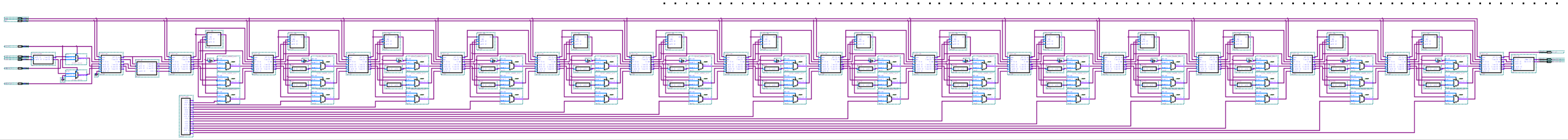
- Run all logic at 56 MHz
- Uses almost half as many FPGA Logic Elements
- Streamlined compared to past architectures

FPGA Resources:
6.8k LE
18 9-bit DSP Blocks

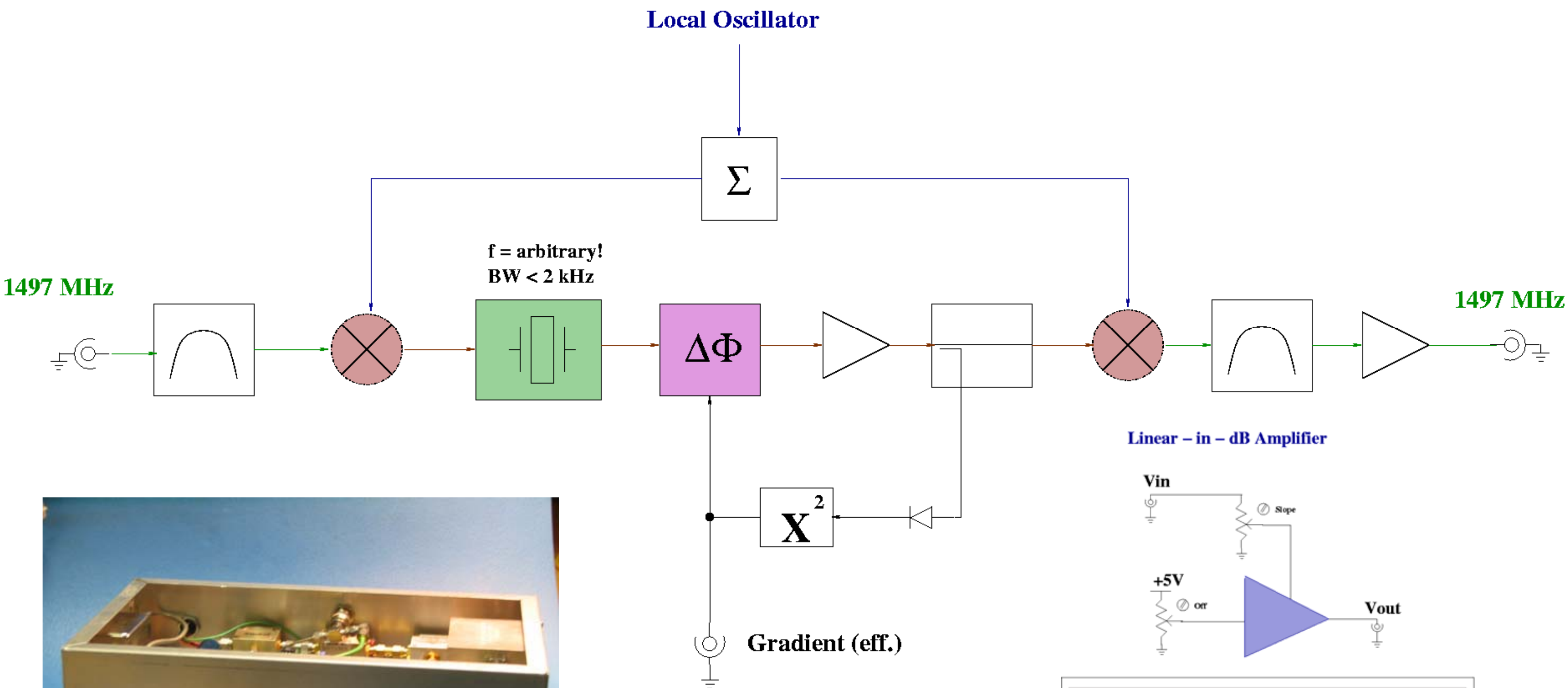
"Tornado"

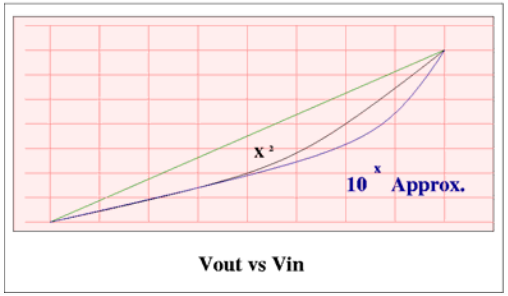
- Pipelined
  - Full data rate
  - 28 MHz I&Q and/or Mag&Phs pairs
  - 56 MHz clock
- Latency
  - One-way 16 clocks at 56 MHz = 285 nsec
  - Both ways 570 nsec



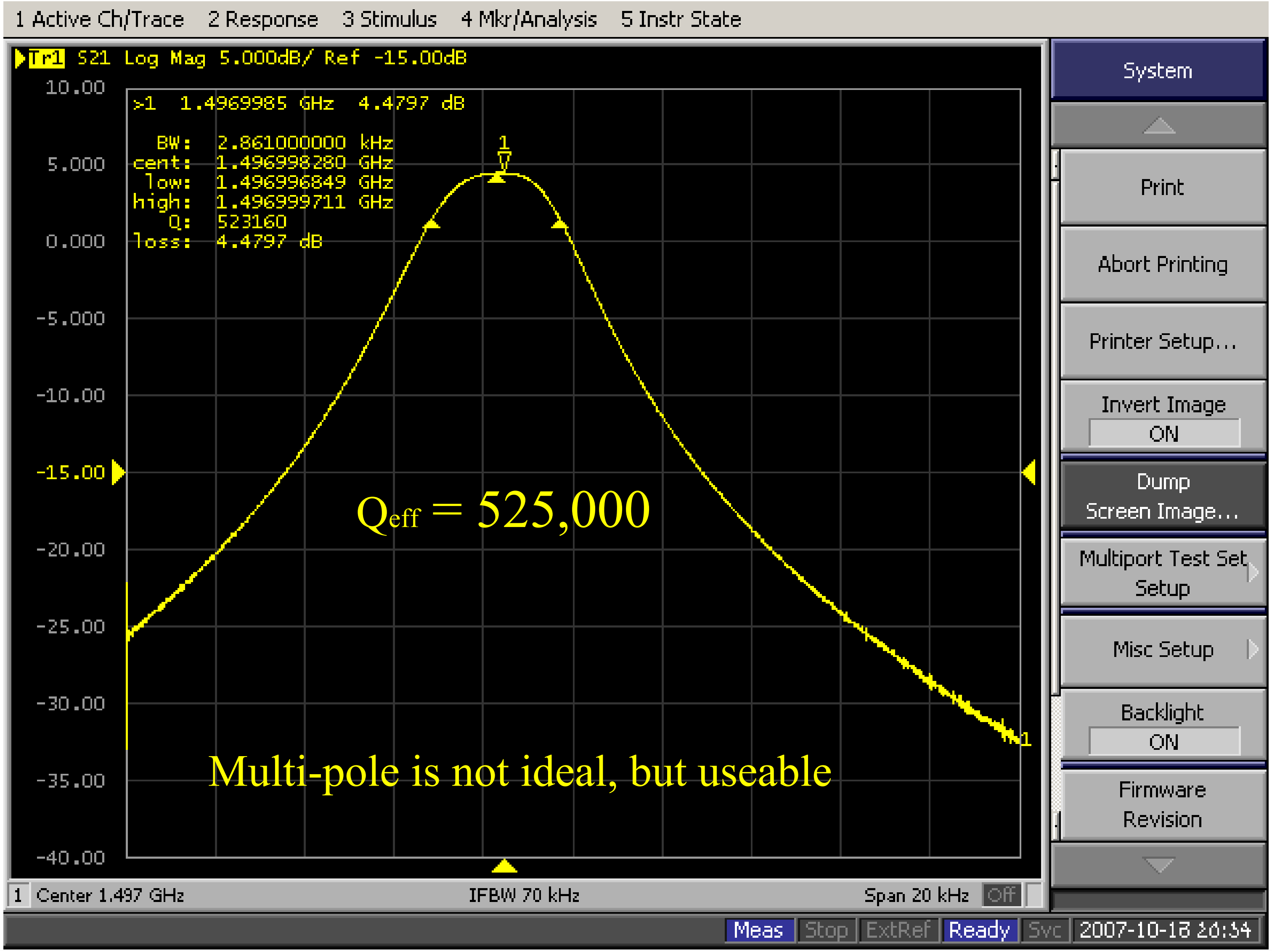


Cavity Emulator



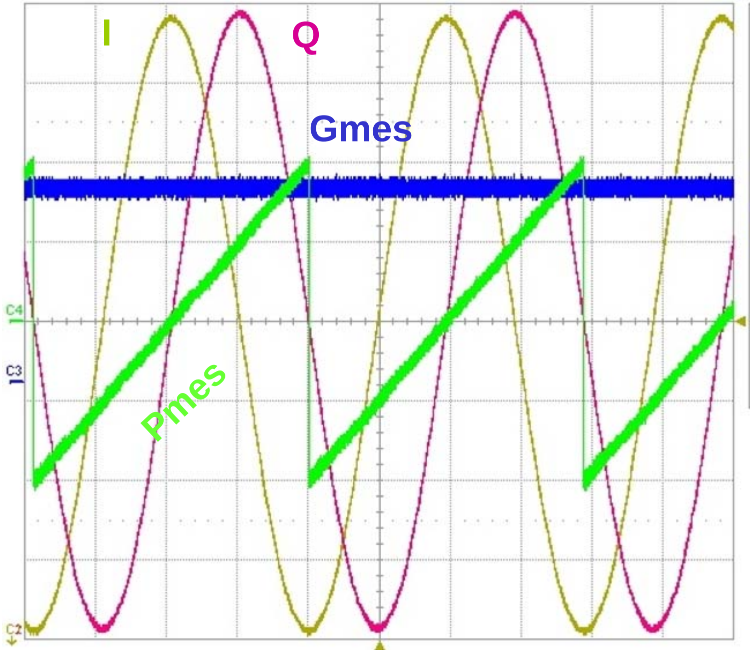


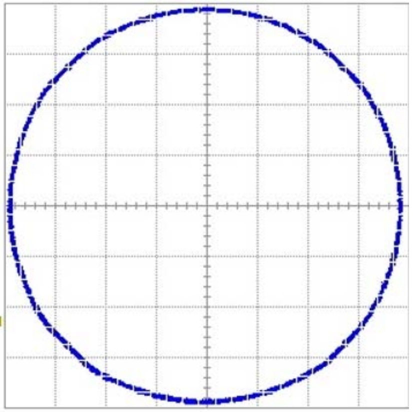
Cavity Emulator (cont.)



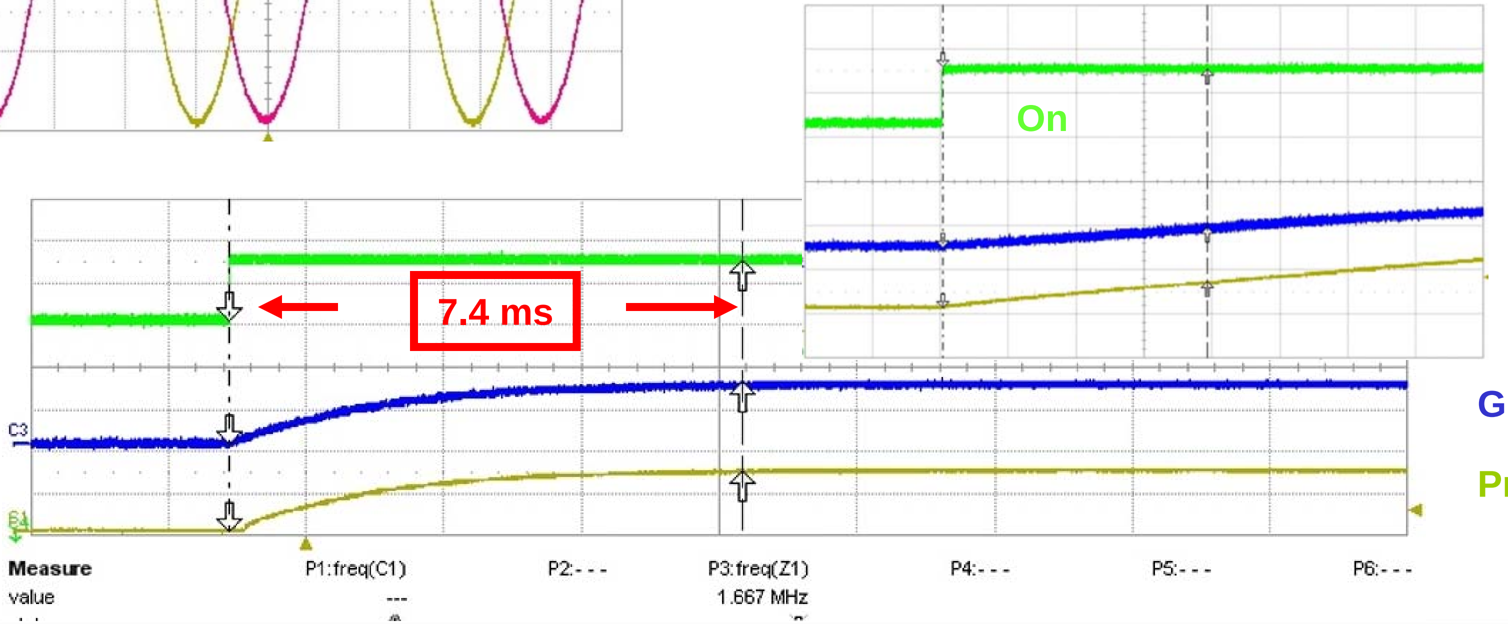
CMTF Results…21 MV/m!

Steady State



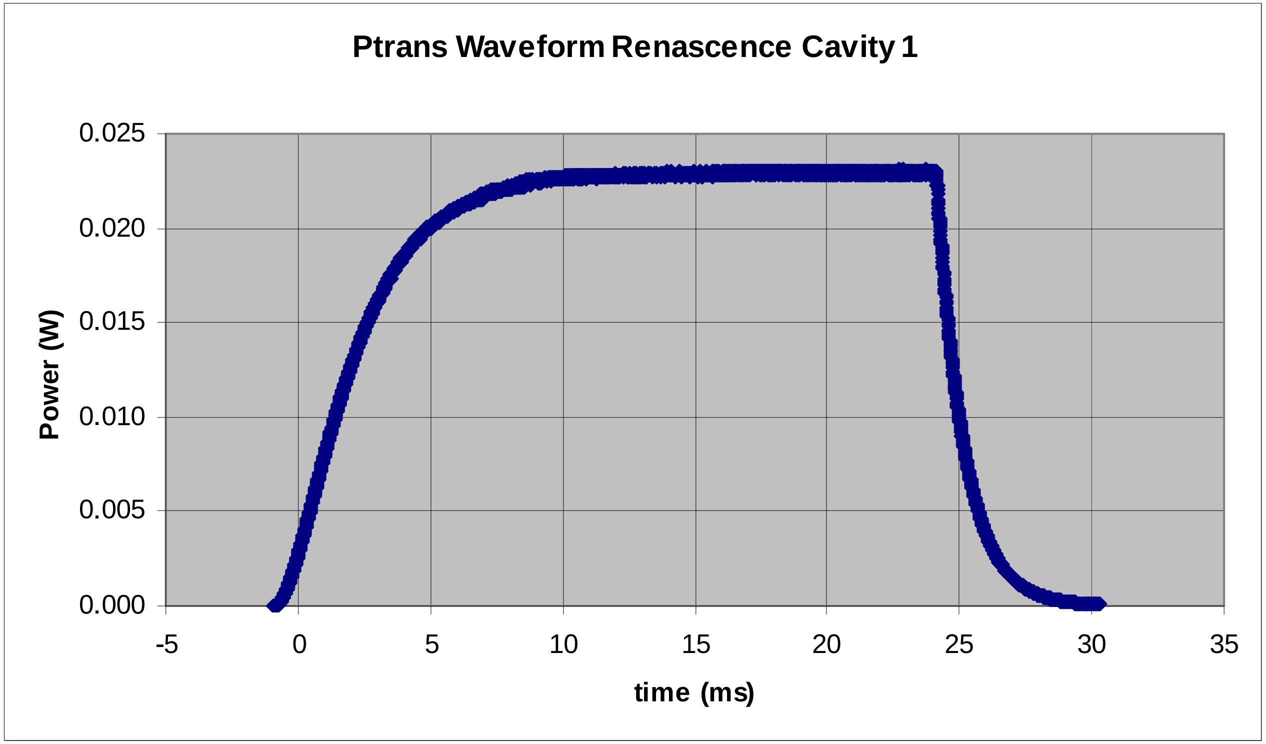


21 MV/m
Turn-on



Gmes
Probe

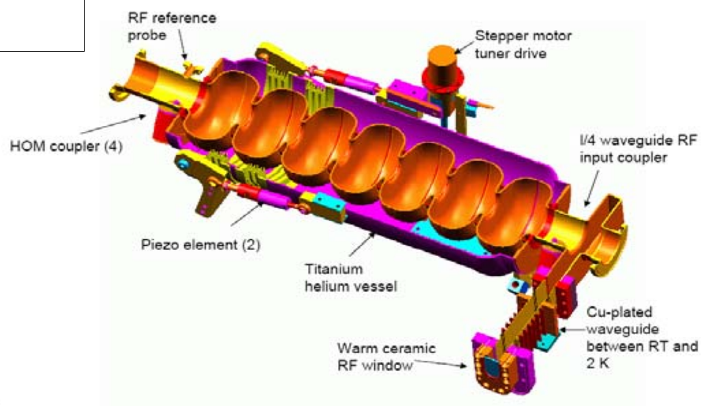
Fill Time, Renascence Cavity 1



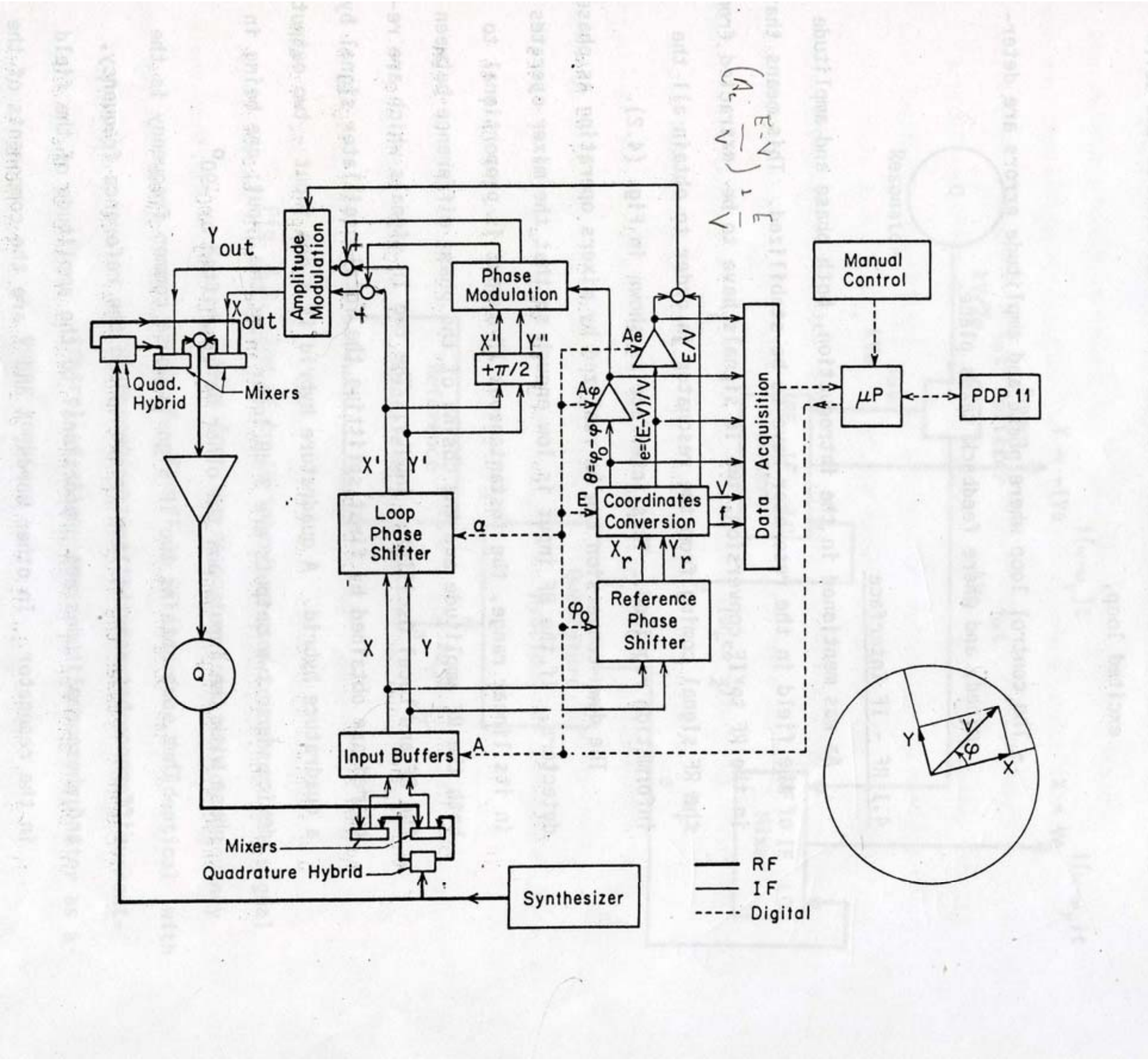
JLAB SRF Institute

CMTF Test Data

Data courtesy of M. Drury, JLAB SRF Institute



Compensation vs. Regulation



Courtesy J.R. Delayen
Ph.D. Dissertation

Hybrid Implementation
(PDP-1173!)

A METHOD OF REDUCING DISTURBANCES IN RADIO SIGNALING BY A SYSTEM OF FREQUENCY MODULATION*

BY
EDWIN H. ARMSTRONG

(Department of Electrical Engineering, Columbia University, New York City)

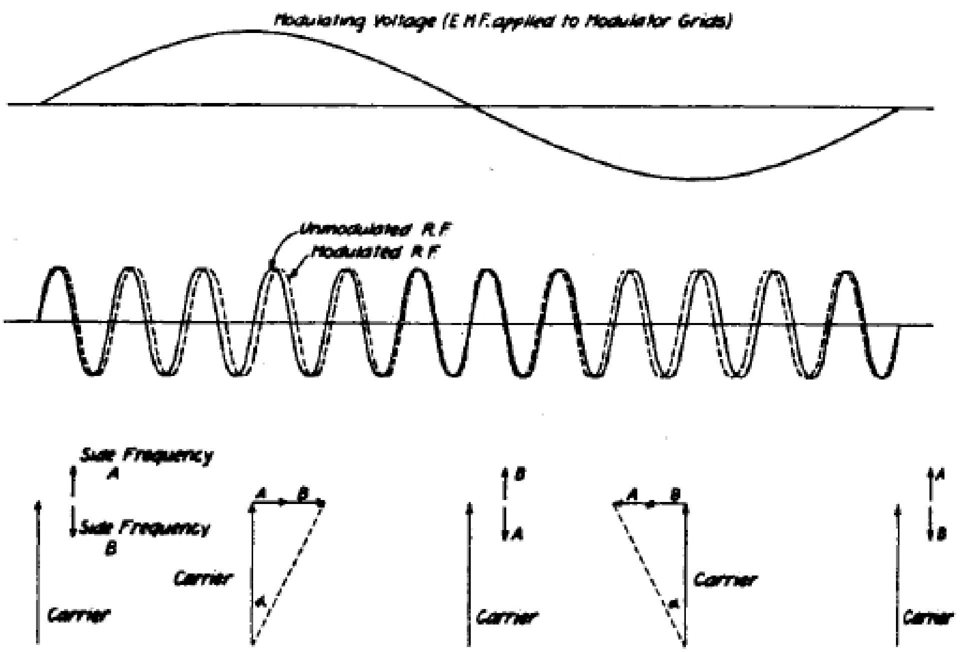
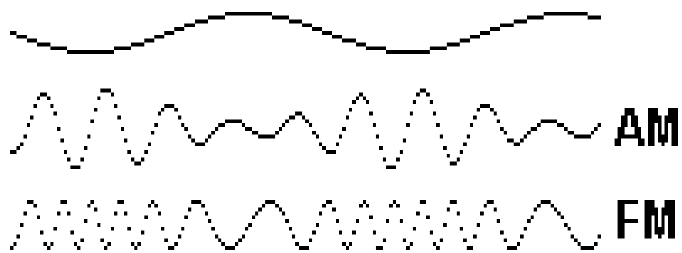
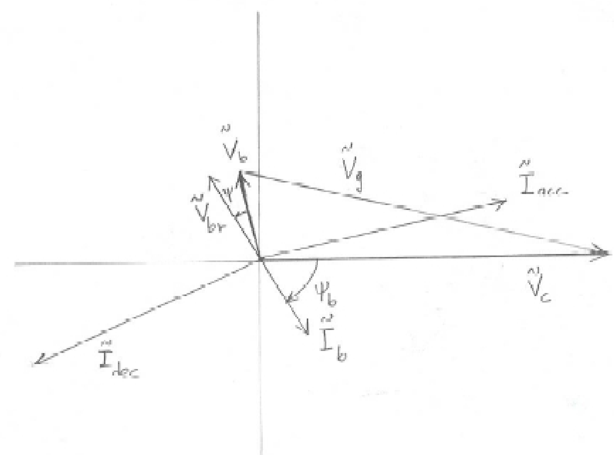


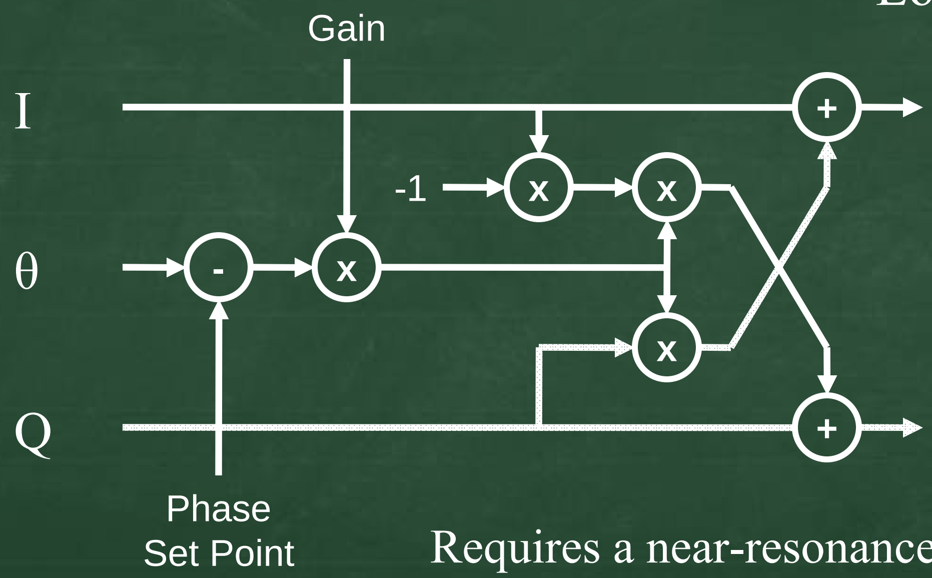
Fig. 3

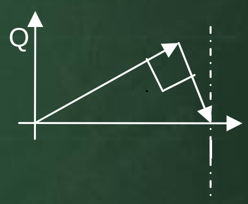




Microphonic Compensation

Add *just enough* quadrature
component to restore amplitude
Lost from cavity envelope…..



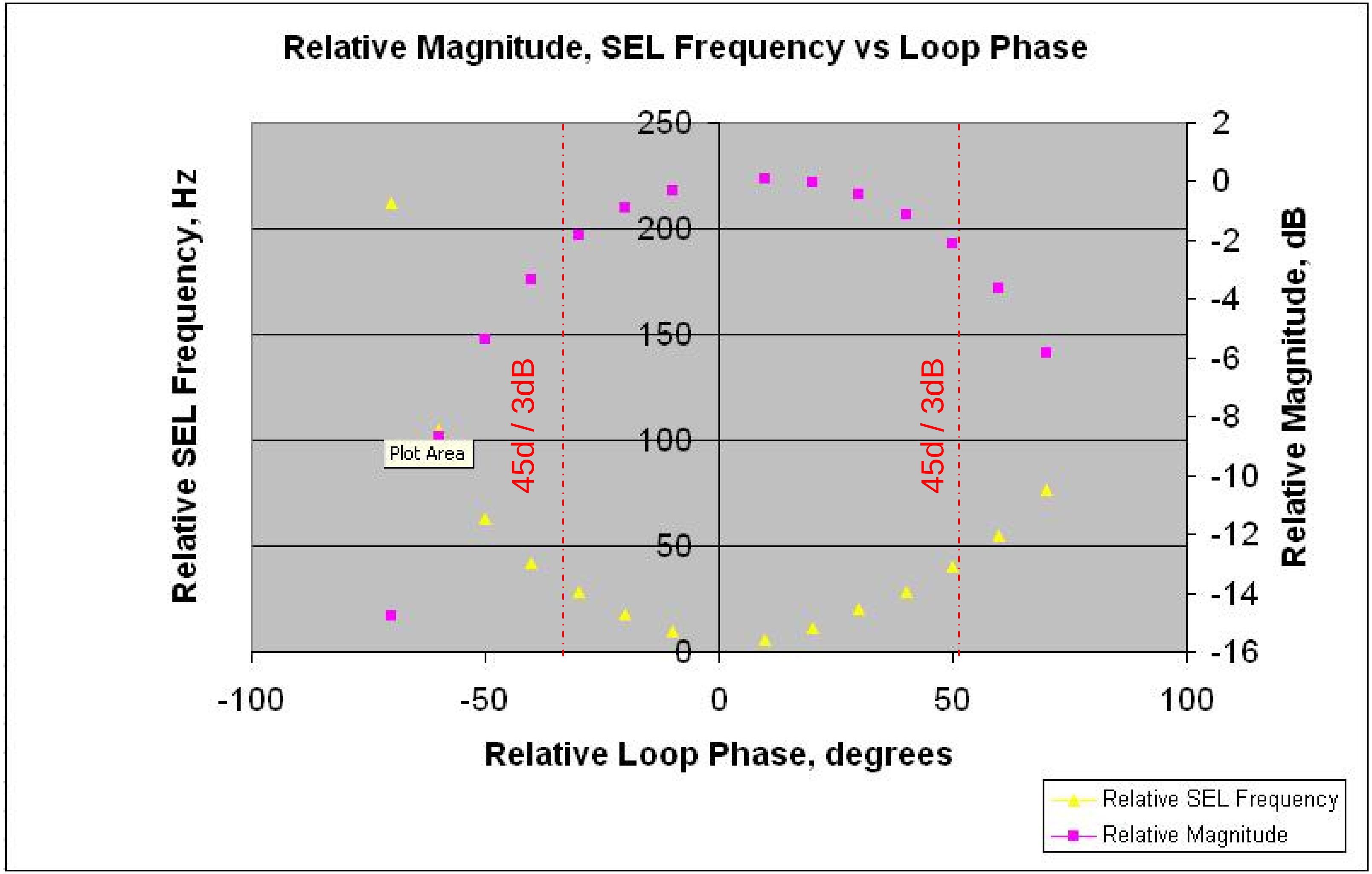


Requires a near-resonance condition:

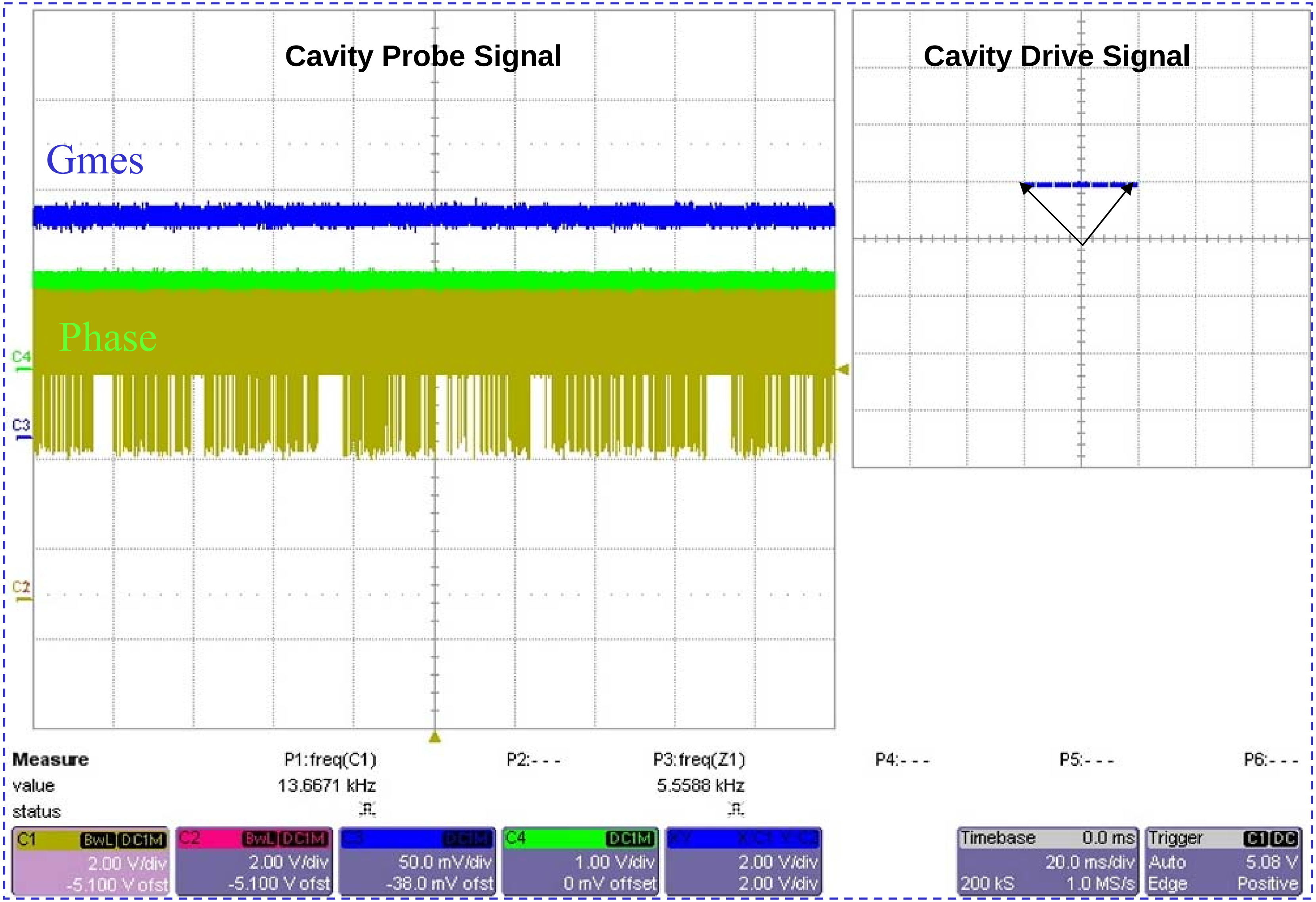
IQ̇-Q İ discriminator, Stepper + Piezo tuners

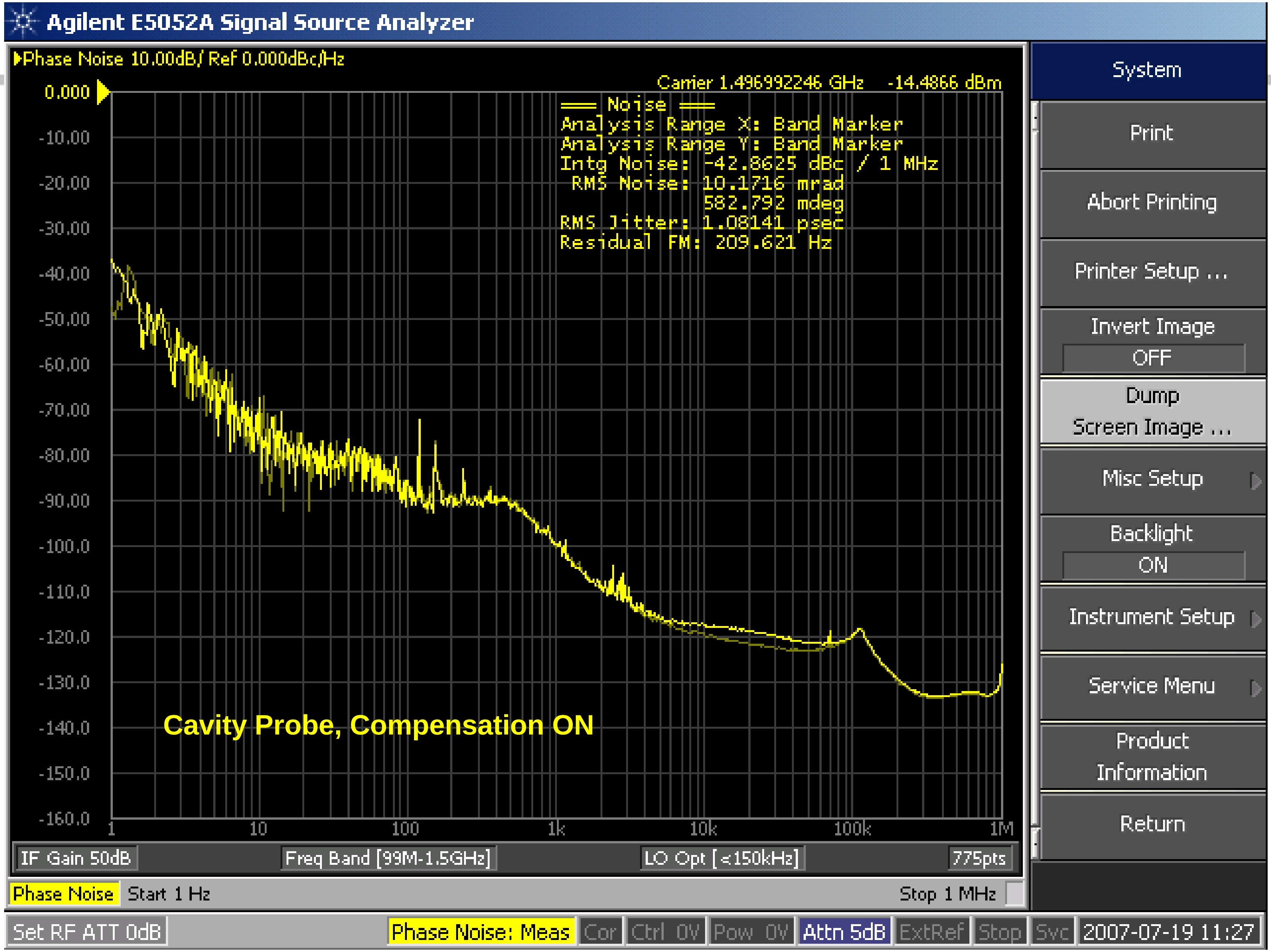
Restoring force results in frequency-lock

Cavity Magnitude vs. SEL Phase (FEL)



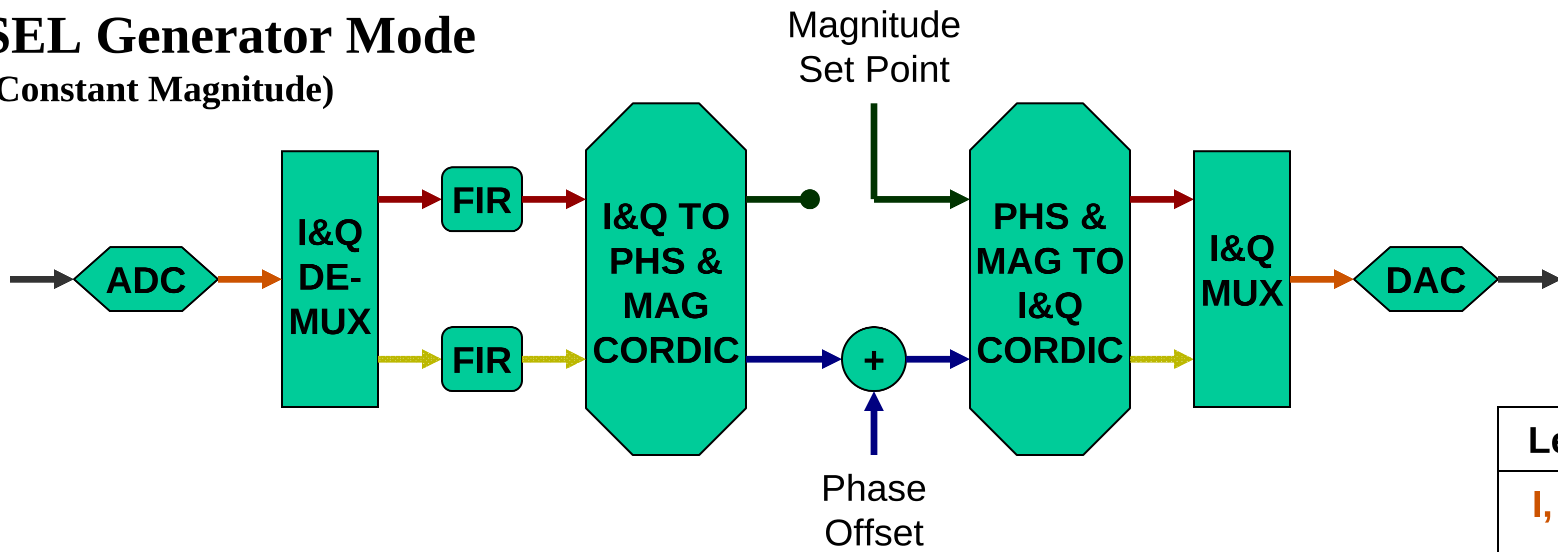
Compensation

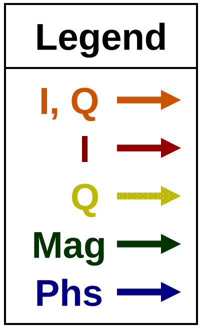



Agilent E5052A Signal Source Analyzer
Phase Noise 10.00dB/ Ref 0.000dBc/Hz
Carrier 1.496992246 GHz -14.4866 dBm
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -42.8625 dBc / 1 MHz
RMS Noise: 10.1716 mrad
582.792 mdeg
RMS Jitter: 1.08141 psec
Residual FM: 209.621 Hz
Cavity Probe, Compensation ON
0.000
-10.00
-20.00
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
-90.00
-100.0
-110.0
-120.0
-130.0
-140.0
-150.0
-160.0
1
10
100
1k
10k
100k
1M
IF Gain 50dB
Freq Band [99M-1.5GHz]
LO Opt [<150kHz]
775pts
Phase Noise
Start 1 Hz
Stop 1 MHz
Set RF ATT 0dB
Phase Noise: Meas
Cor
Ctrl OV
Pow OV
Attn 5dB
ExtRef
Stop
Svc
2007-07-19 11:27
System
Print
Abort Printing
Printer Setup ...
Invert Image
OFF
Dump Screen Image ...
Misc Setup
Backlight
ON
Instrument Setup
Service Menu
Product Information
Return

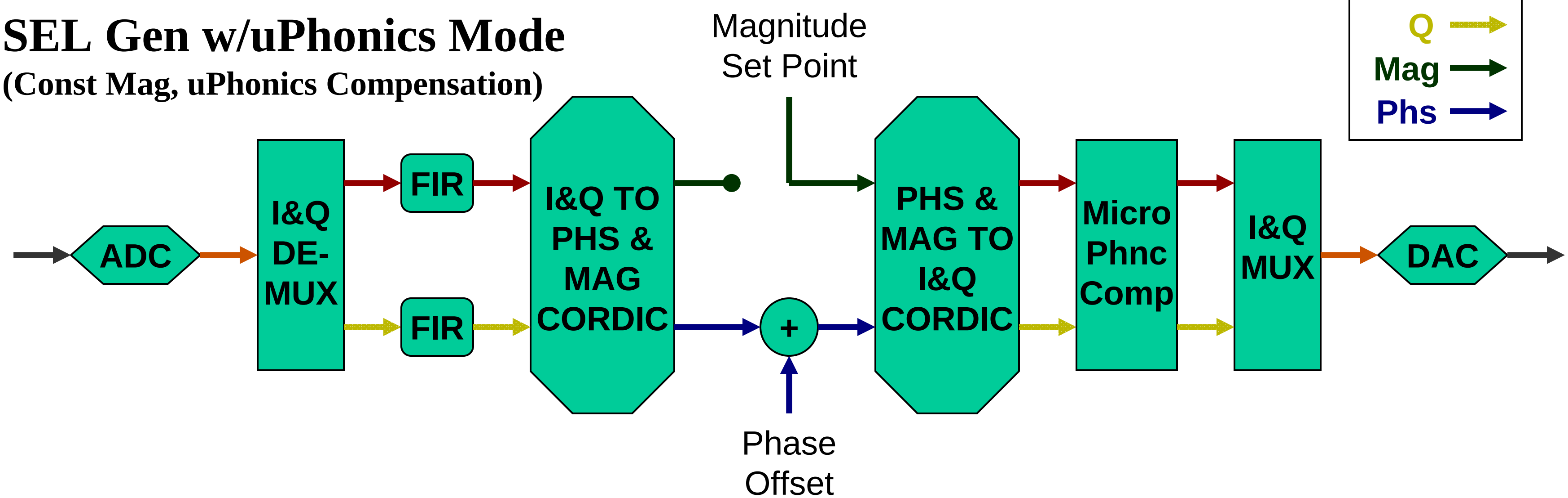
SEL Output Stabilization / Compensation

SEL Generator Mode
(Constant Magnitude)



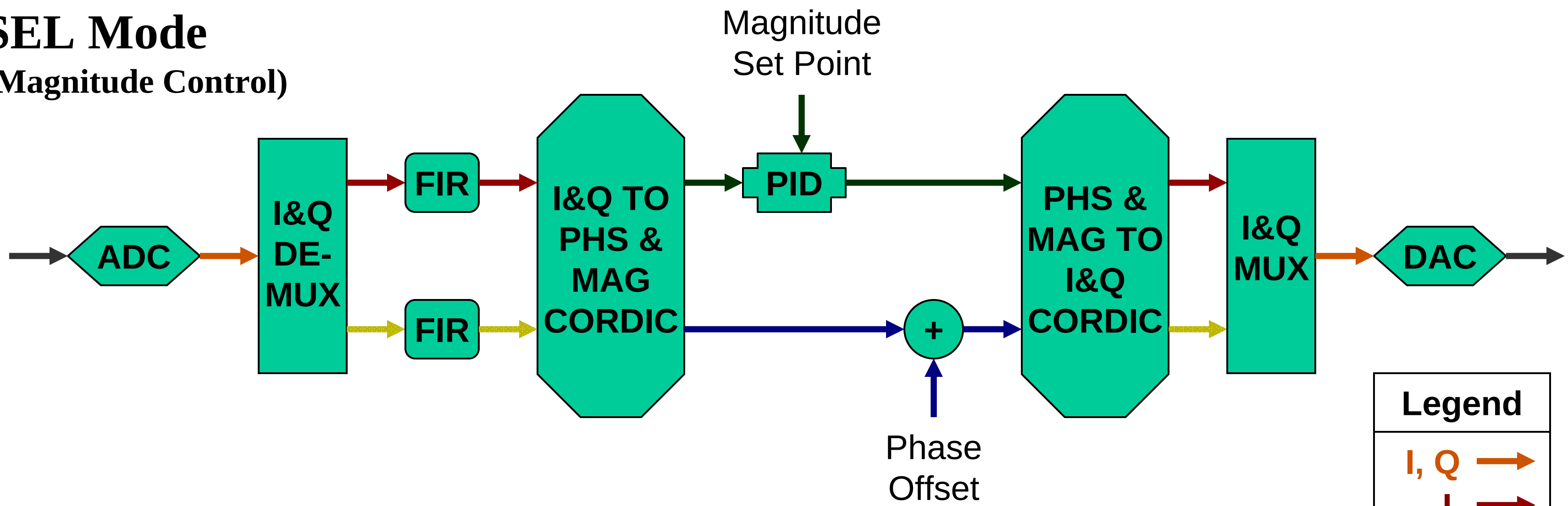


SEL Gen w/uPhonics Mode
(Const Mag, uPhonics Compensation)

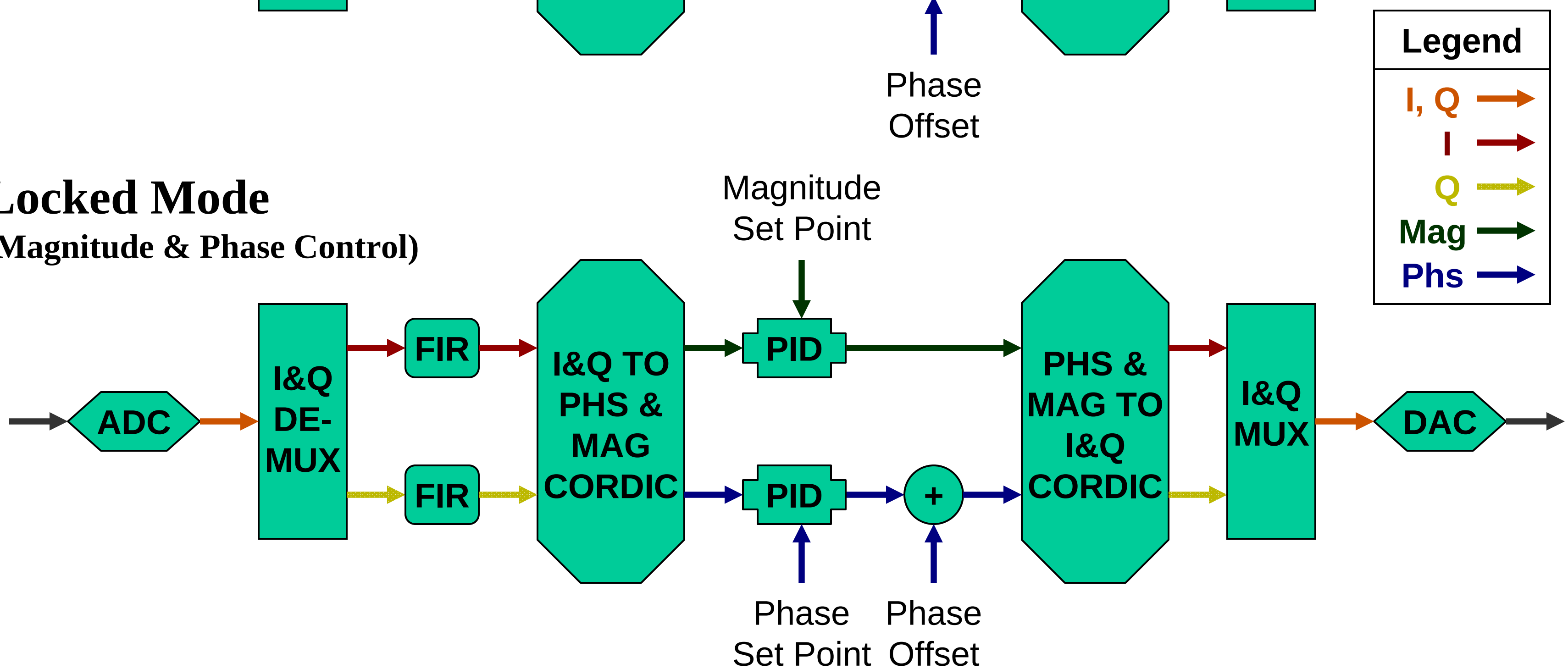


Phase 2: PID SEL Input Regulation

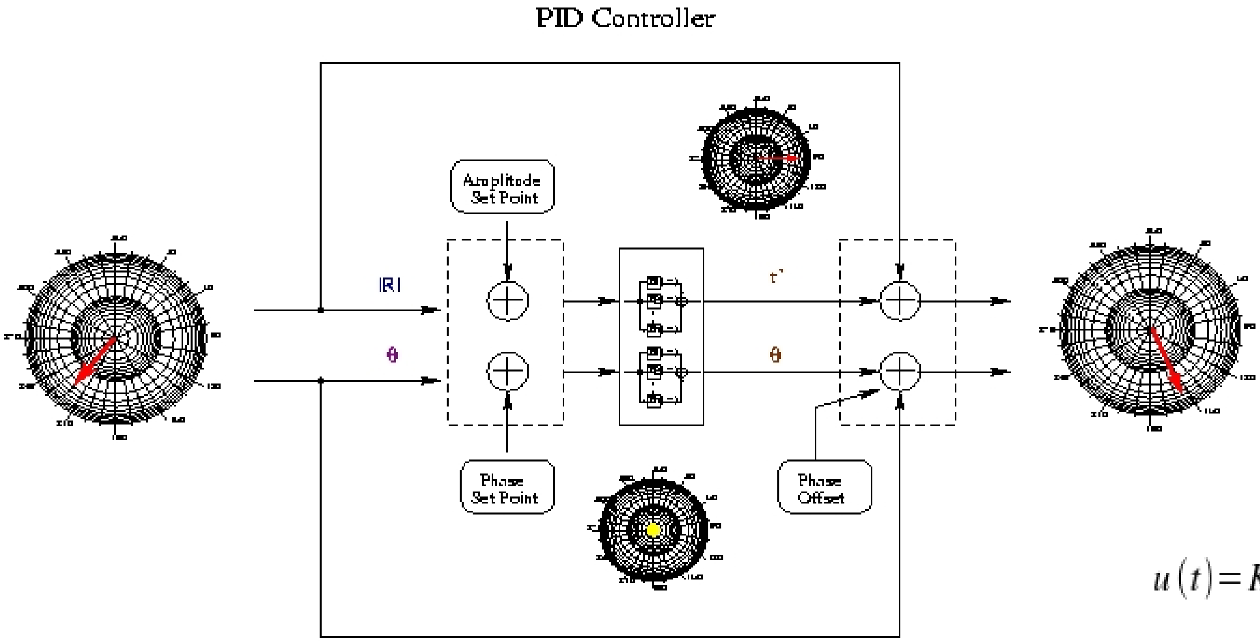
SEL Mode
(Magnitude Control)



Locked Mode
(Magnitude & Phase Control)



PID Controller…WIP



Linear path + non-linear path

$$u(t) = Kp \cdot e(t) + Ki \cdot \int e(T)\,dT + \frac{Kd \cdot (de(t))}{dt}$$

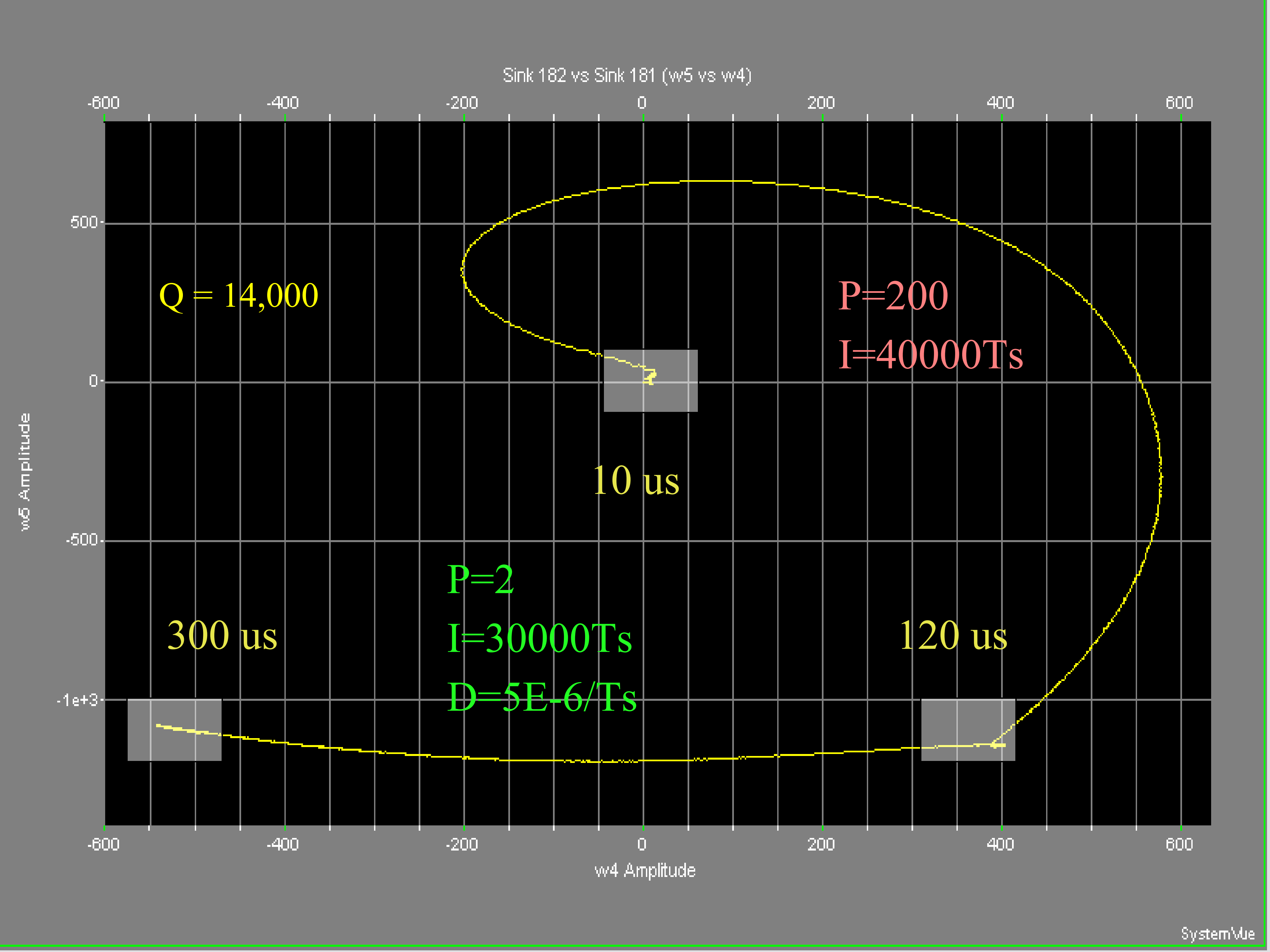
$$u(k) = u(k-1) + K1 \cdot e(k) + K2 \cdot e(k-1) + K3 \cdot e(k-$$

$$K1 = Kp + \frac{TKi}{2} + \frac{Kd}{T}$$

$$K2 = -Kp - \frac{2Kd}{T} + \frac{TKi}{2}$$

$$K3 = \frac{Kd}{T}$$

$$T = \frac{1}{fs}$$



Sink 182 vs Sink 181 (w5 vs w4)
-600
-400
-200
0
200
400
600
500
0
-500
-1e+3
w5 Amplitude
w4 Amplitude
Q = 14,000
P=200
I=40000Ts
10 us
P=2
I=30000Ts
D=5E-6/Ts
300 us
120 us
SystemVue

Summary

Successful all-digital SEL implementation for 21MV/m cavity system!

Demonstration of amplitude compensation, for near-resonance

Hardware not linked to application….truly SDR architecture

MATLAB modeling = AHDL Modeling, bit-for-bit

MATLAB dynamic cavity model in incubator

Cavity emulator useful for bench testing

SEL Self-starts easily