

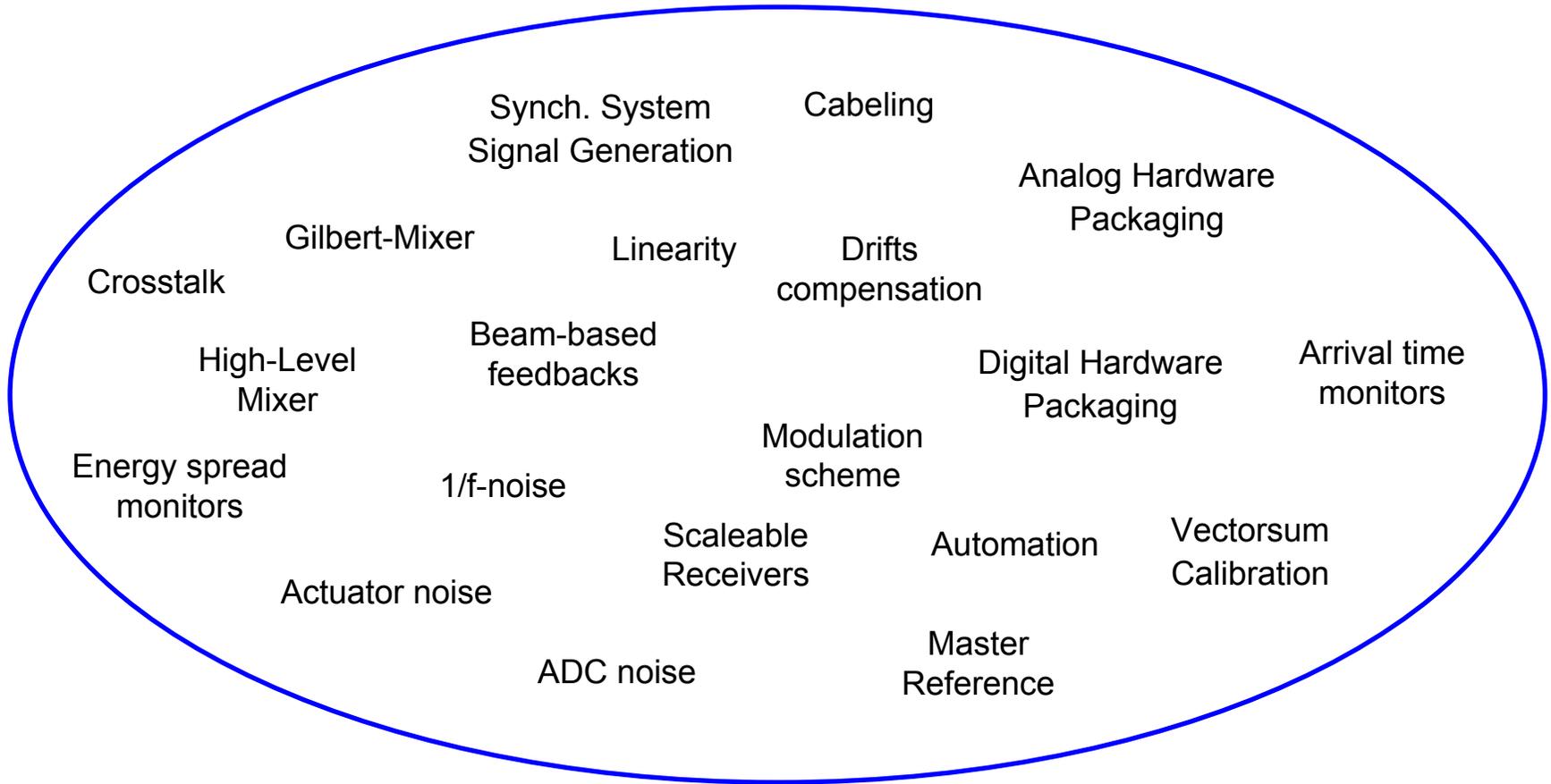


Survey of Receiver Hardware and Techniques'

- Frank Ludwig / DESY -

Content :

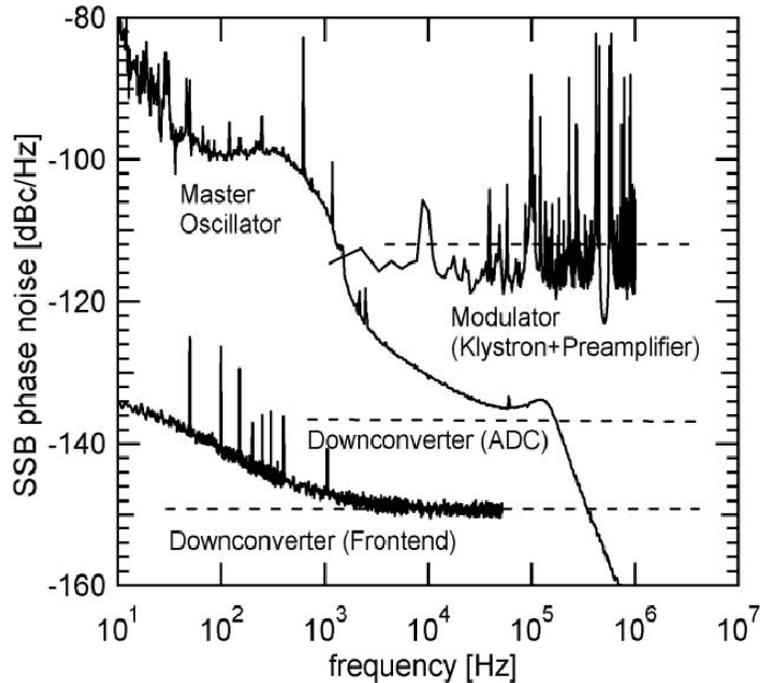
- 0 Motivation
- 1 Survey of Receiver and Hardware techniques
 - IQ Sampling (switched LO signal)
 - IF Sampling + Digital down conversion (RF down conversion)
 - Direct Sampling
 - (Baseband sampling (analog IQ detection))
- 2 Beam stability measurements
- 3 Summary and Outlook



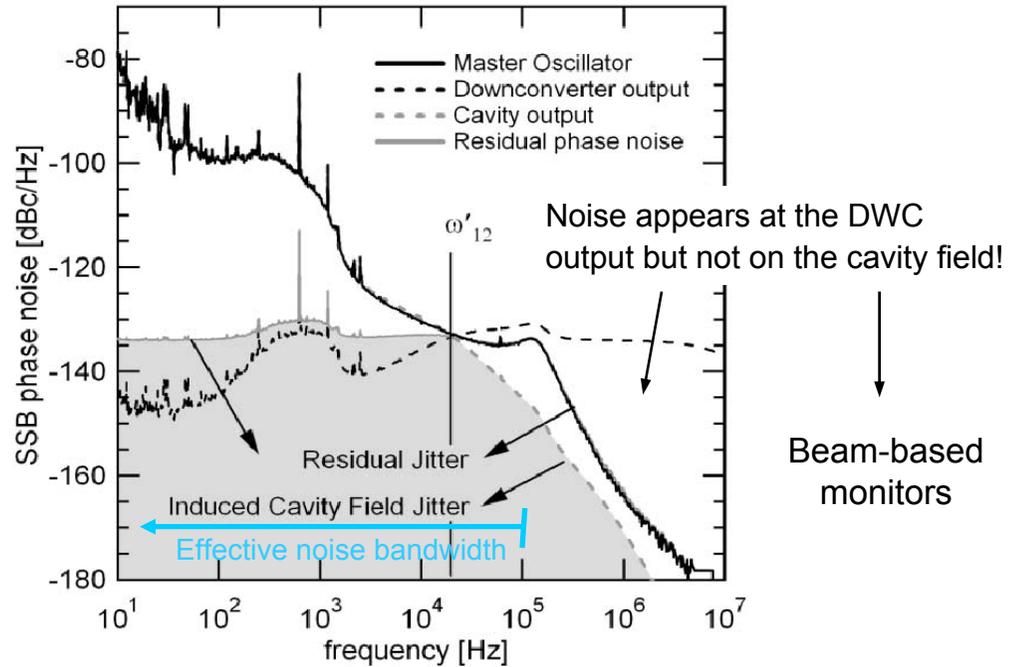
What is most important for a beam stability significantly lower than 0.01% ?

Phase noise budget at FLASH (Switched LO, single cavity)

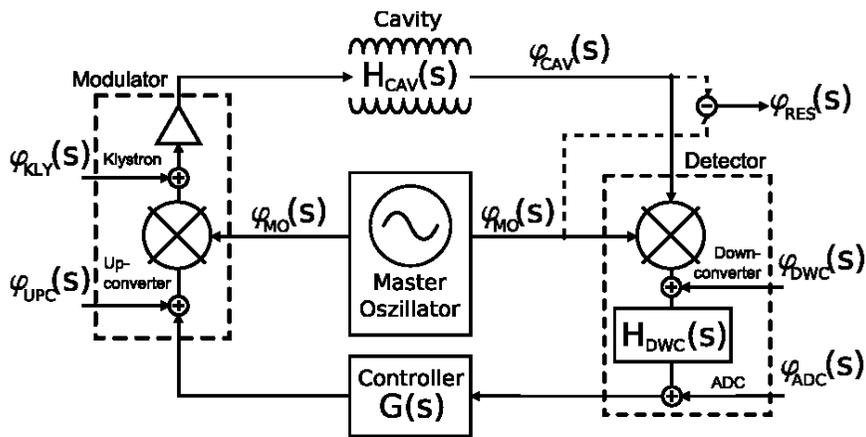
Phase noise measurements :



Contributions to cavity field jitter :



Beam-based monitors



Subsystem	Phase noise [dBc/Hz]	Residual jitter [fs]	Induced jitter [fs]
MO	see Fig.3	14.1	5.5
DWC (Frontend)	-147	1.8	1.8
DWC (ADC)	-135	5.8	5.8
MOD	-110	1.2	1.2

(Complete ADC module)

- High frequency noise is filtered by the cavity, but not drifts or 1/f-noise!
- Beam relevant frequency range [1Hz, 100kHz]

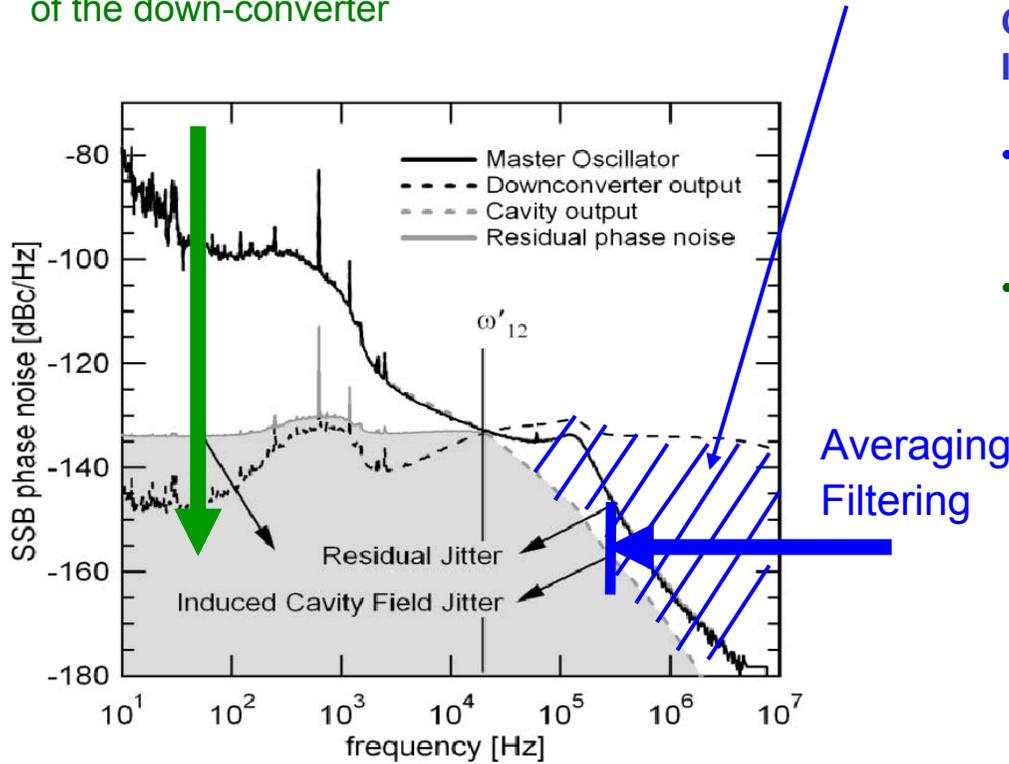
„Beam performance“:

Increase SNR by

- Increase input power vs. linearity
- Decrease noise spectral density of the down-converter

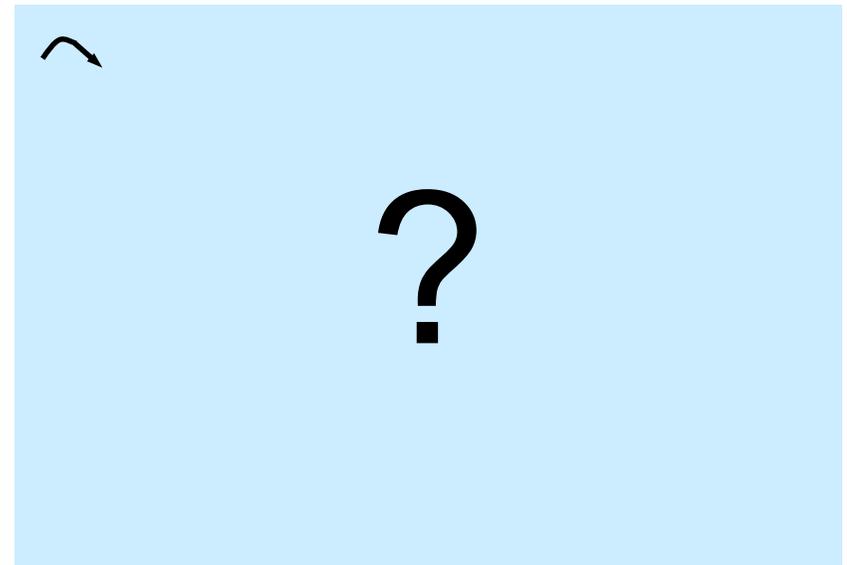
„Display property for the operator“:

Noise appears at the DWC output but not on the cavity field!

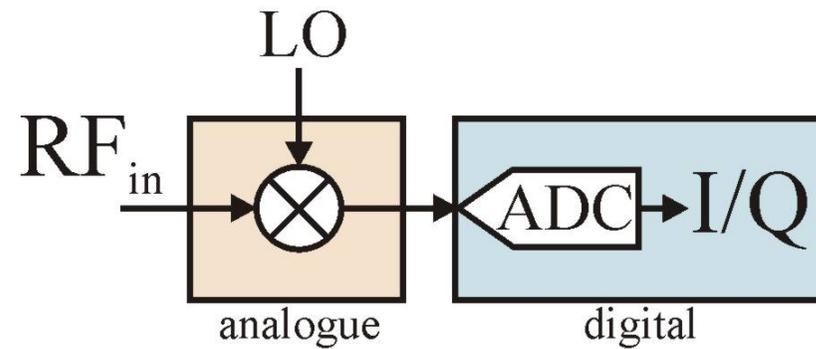


Choice of sampling method (minor problem):
IQ sampling system → [1,50] MHz CW system

- gives together with the high ADC sampling rate the possibility of averaging (reduces noise at high frequencies mainly for the „display“)
- Increase input power, reduce mixer post amplification and fulfill linearity condition for the vectorsum calibration



IQ sampling scheme



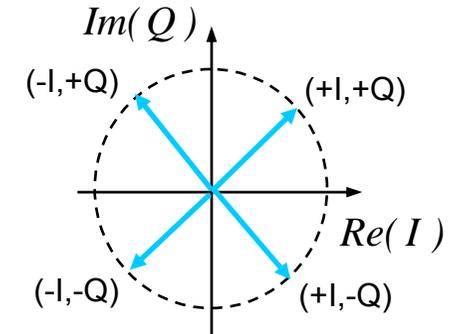
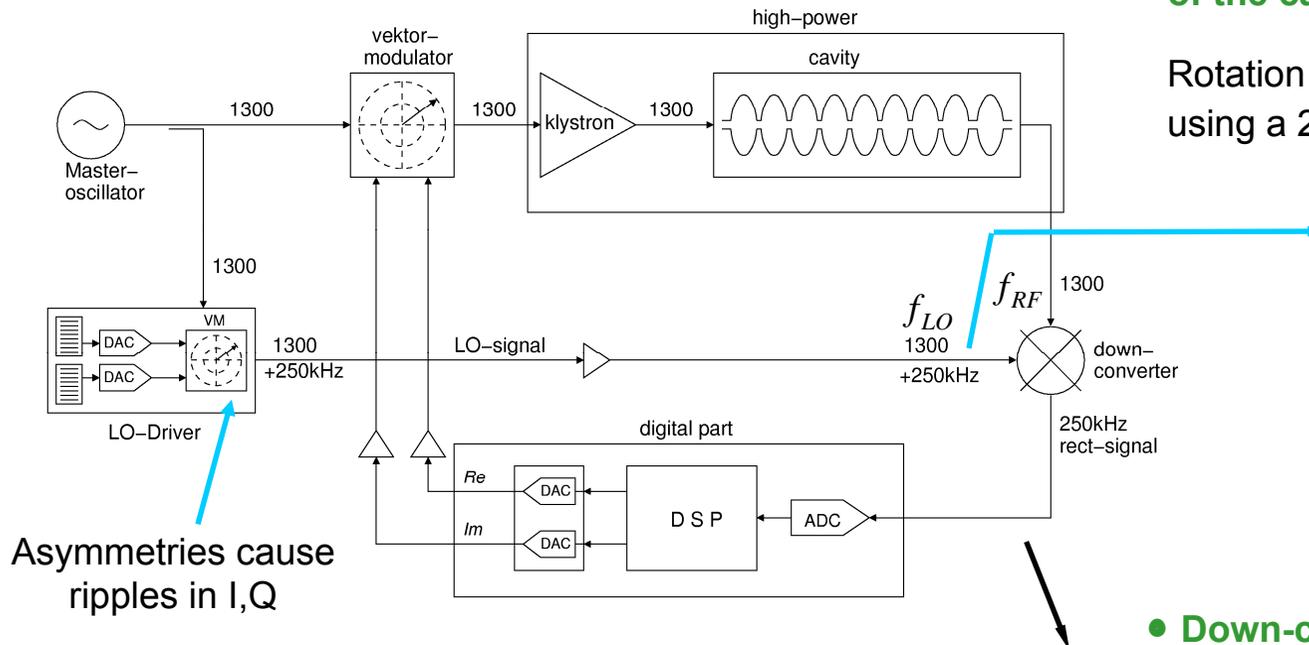
(Courtesy of T.Schilcher/ PSI – CAS)

IQ sampling scheme in practice

● **Actual LLRF control system using a switched LO-signal :**

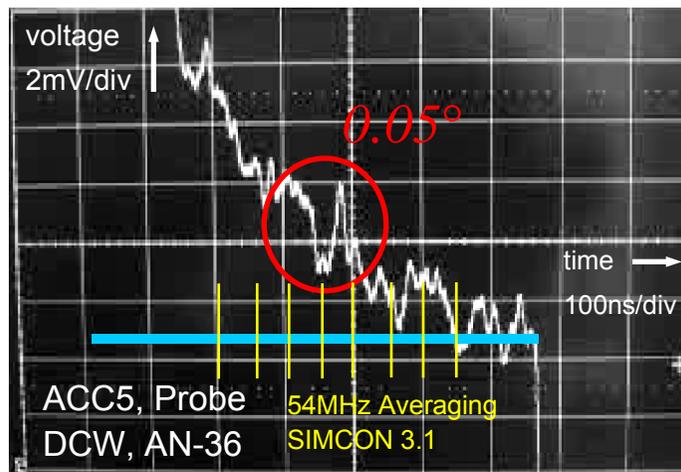
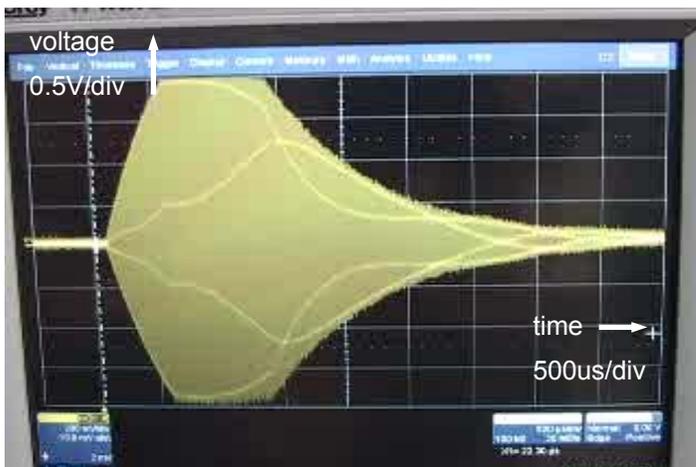
● **Phase and amplitude detection of the cavity field vector :**

Rotation of the LO-signal in four 90° steps, using a 250kHz squared LO-Signal.



Asymmetries cause ripples in I,Q

● **Down-converter output IF-signal :**



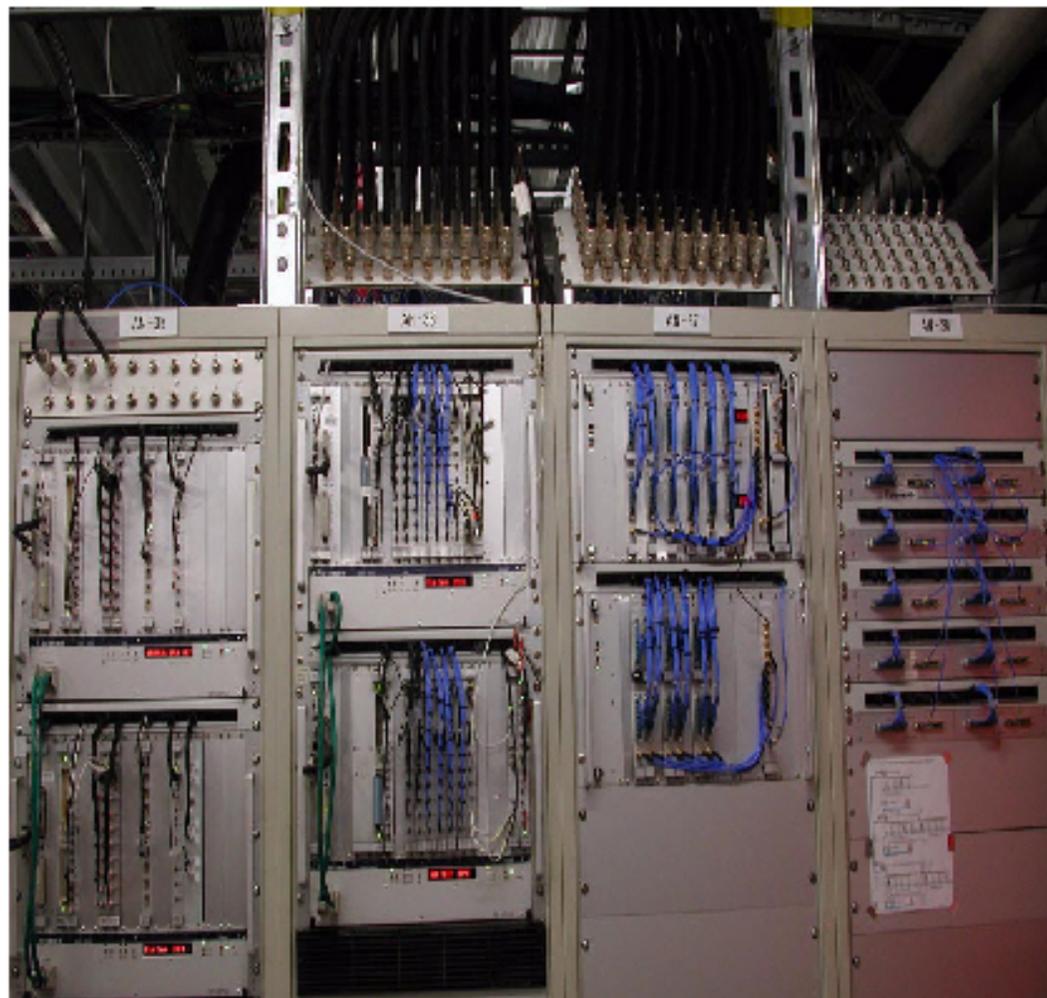
Bandwidth for transforming 250kHz squared pulses :
 $\Delta f \approx 10\text{MHz}$

but required regulation bandwidth is only :
 $\Delta f \approx 1\text{MHz}$

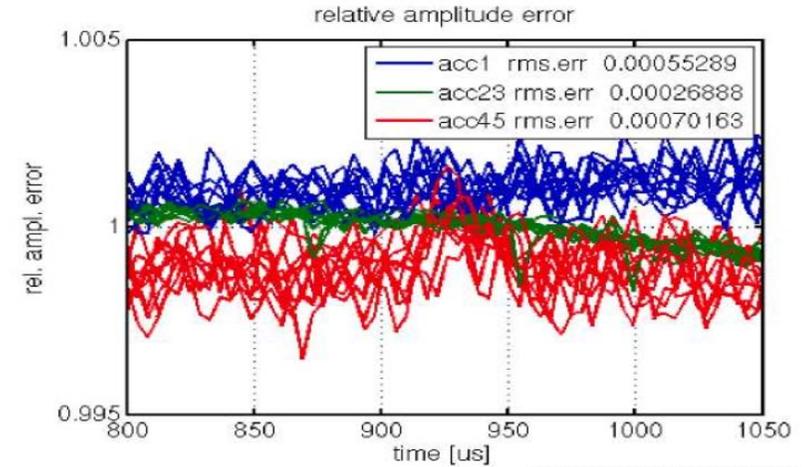
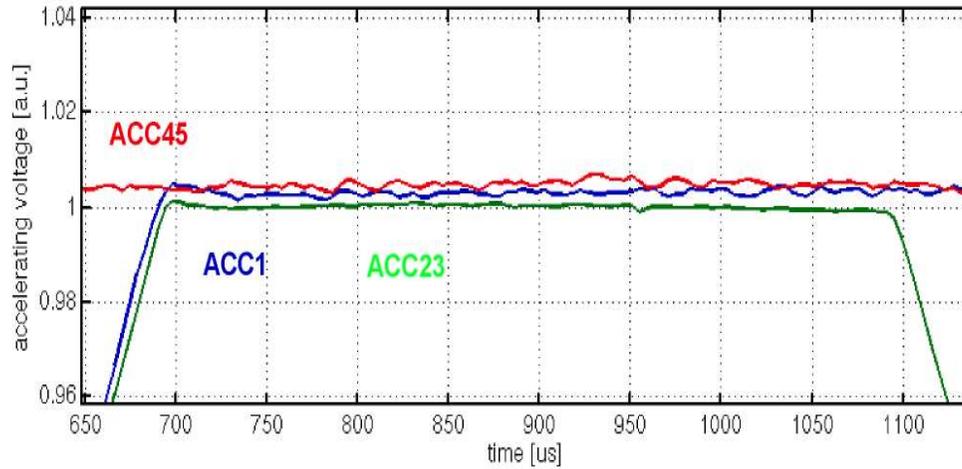
Gun and ACC1



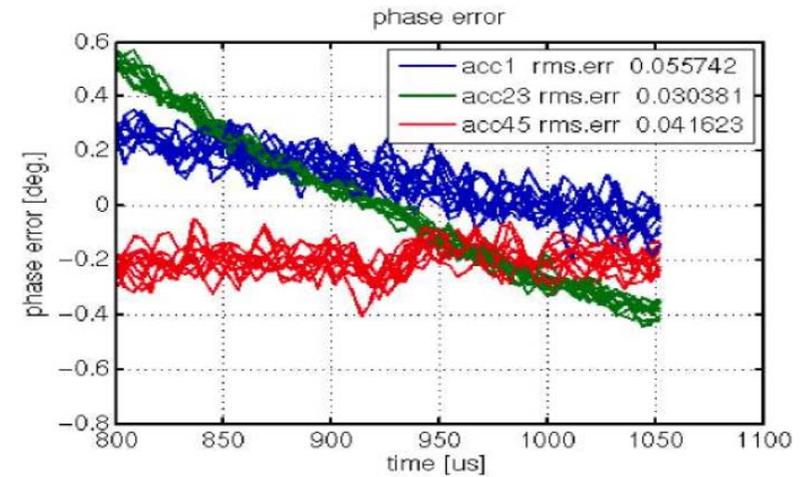
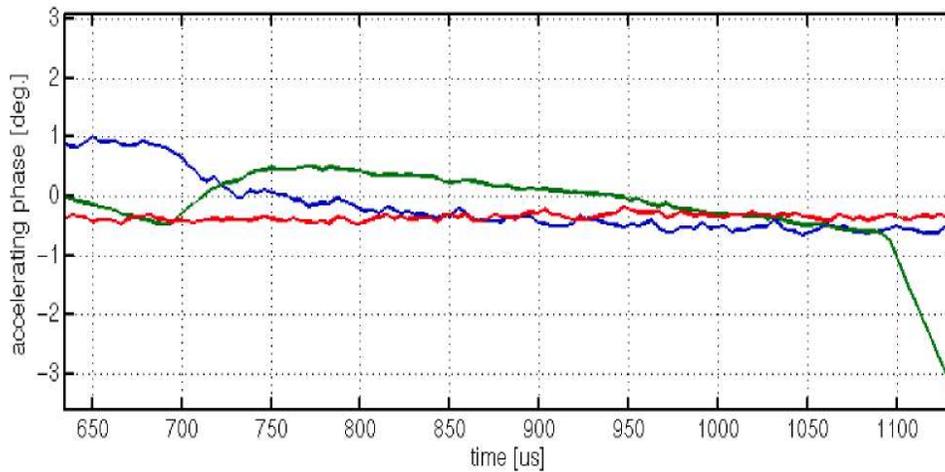
ACC2, ACC3, ACC4 & ACC5



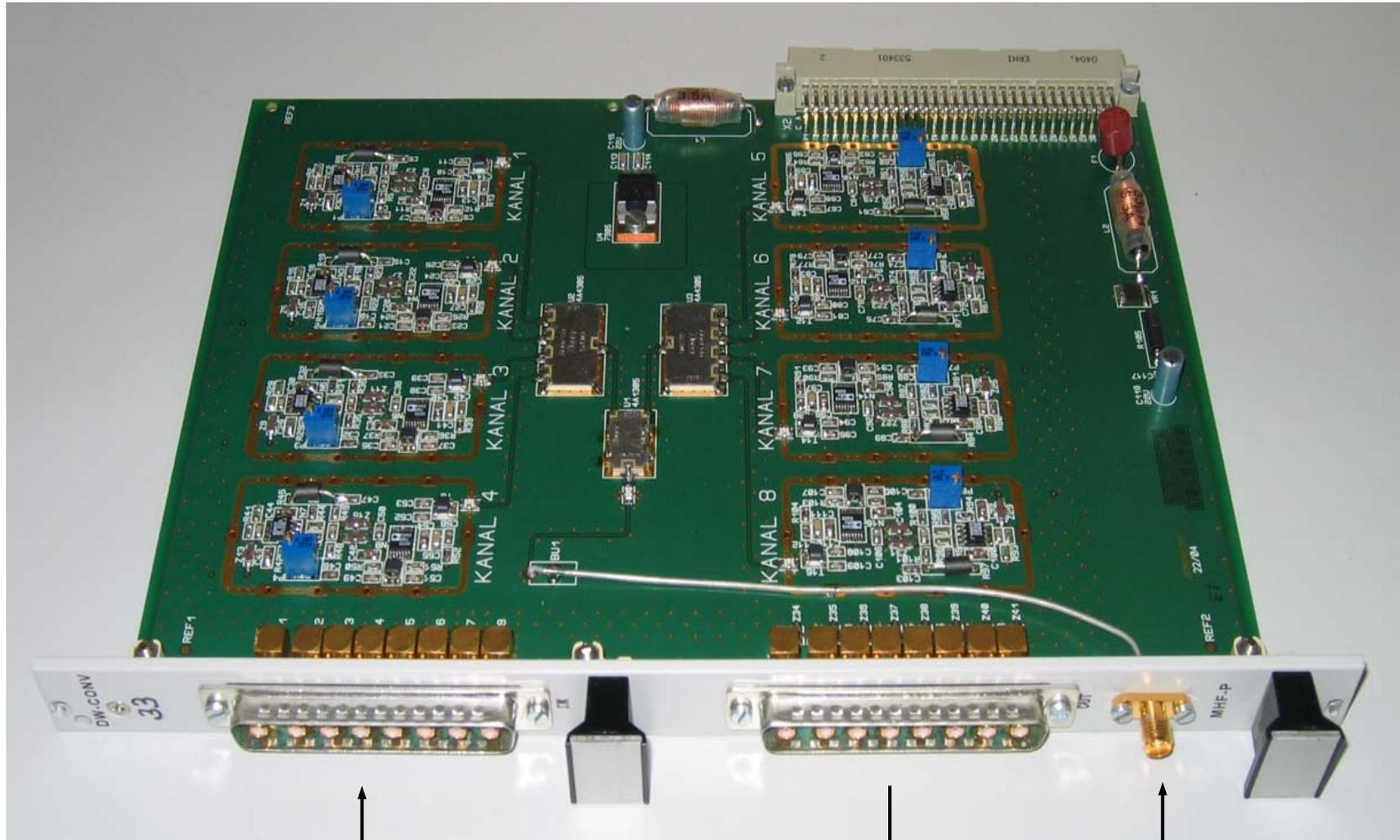
- Performance of the 250kHz IQ Sampling scheme at FLASH :



$$\delta A / A \approx 2 \cdot 10^{-4} \dots 7 \cdot 10^{-4}$$



$$\delta \varphi \approx 0.03 \dots 0.05^\circ$$



8-channels from cavity probe :

$$P_{RF} \approx [-40 \text{ dBm}, -10 \text{ dBm}]$$

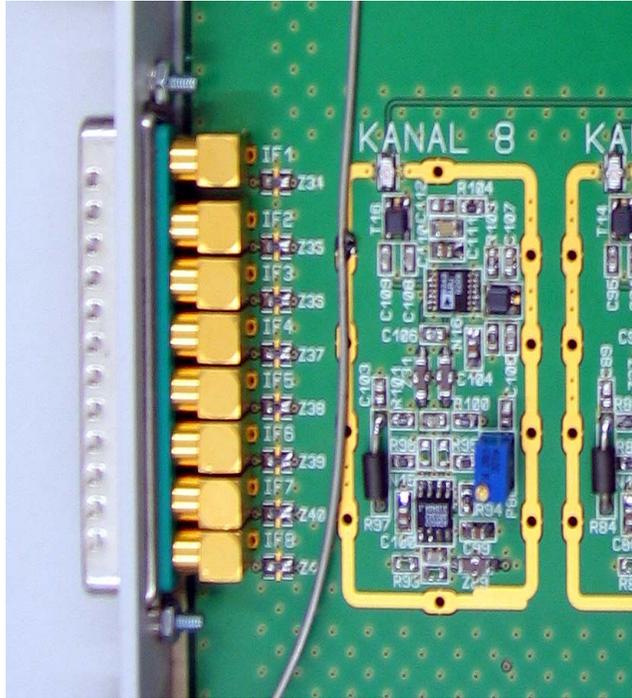
8-channels to ADC-Board :

$$\sqrt{S_U} \approx 70 \text{ nV} / \sqrt{\text{Hz}}$$

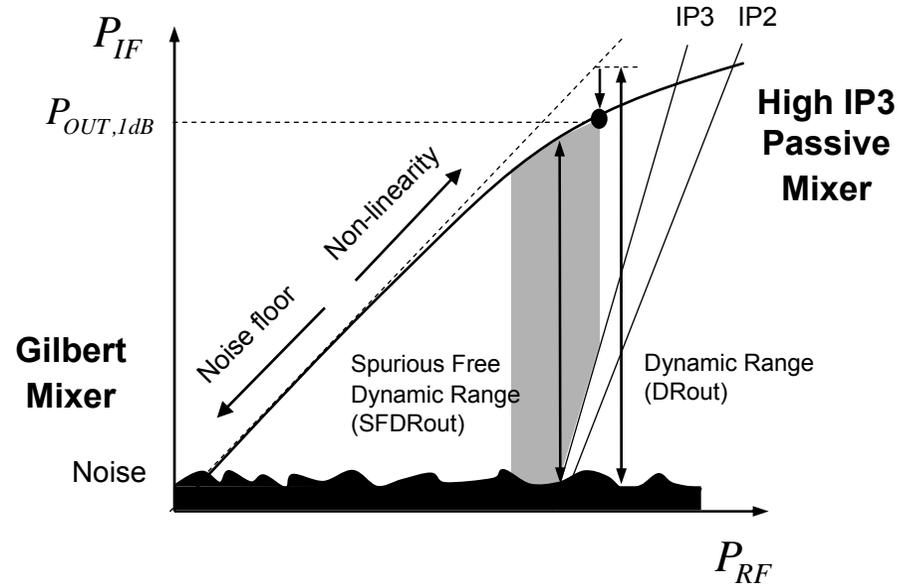
LO-Input :

$$P_{LO} \approx -5 \text{ dBm}$$

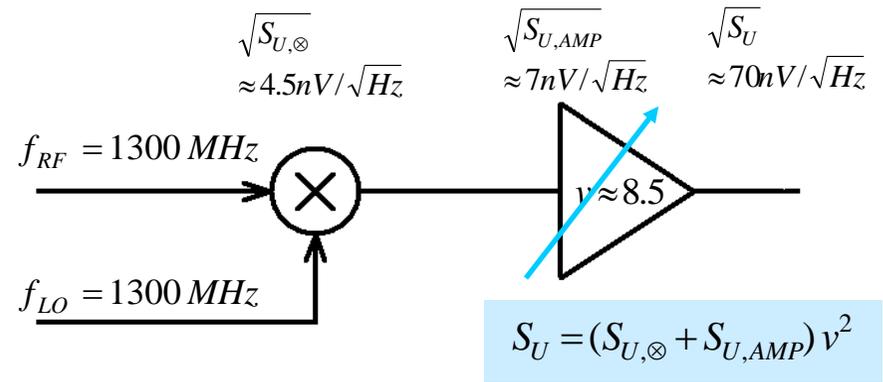
Actual multichannel down-converter



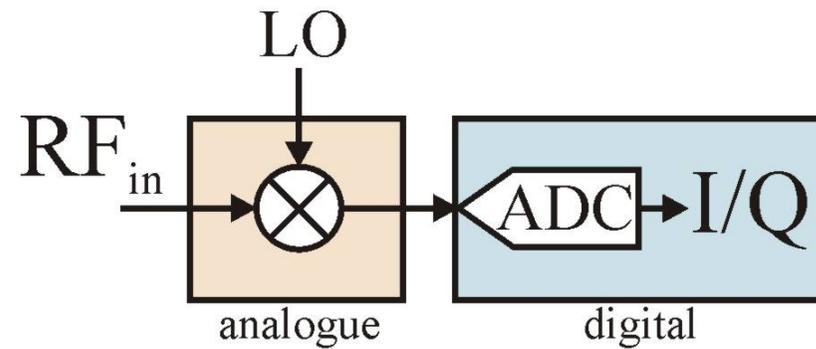
• **Compromise between noise and linearity :**



- Second amplification determines performance
 - Expected down-converter performance from baseband measurements:
- $(\Delta A / A) \approx 0.2 E - 4 \approx 0.2 \delta U_{XFEL}$, (Cavity filtered)
 $\Delta f = 100 \text{kHz}$,

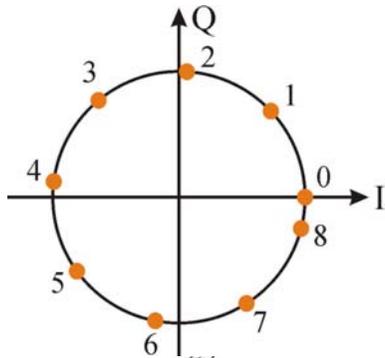
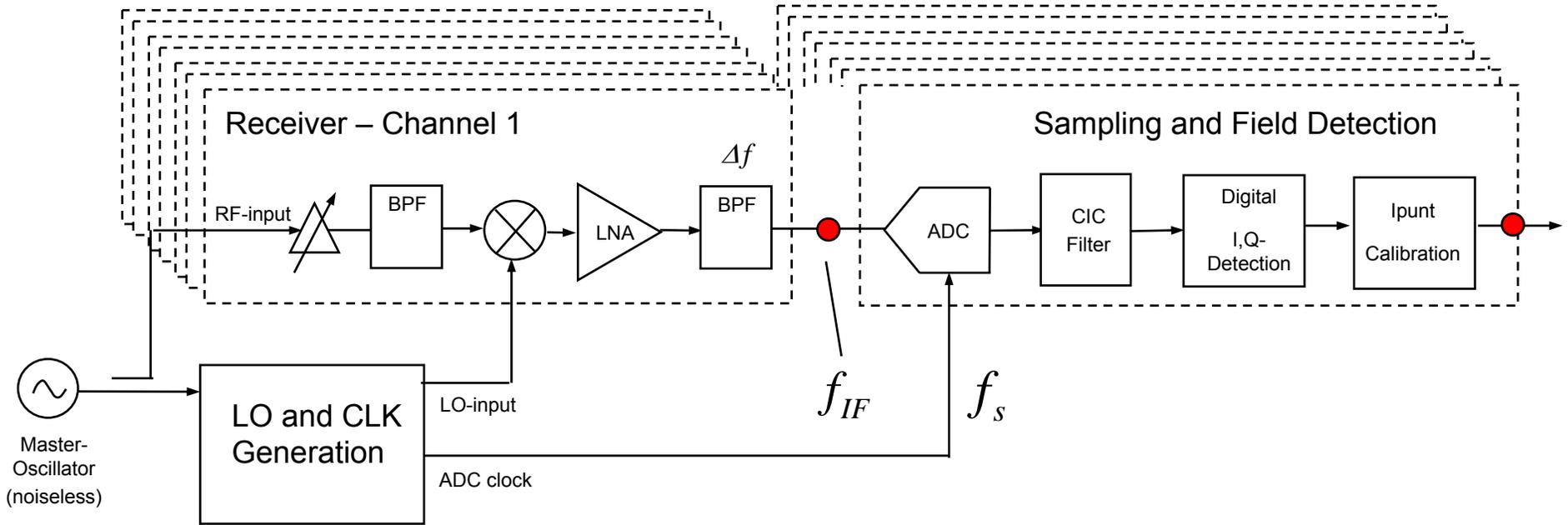


IF sampling scheme (non-IQ sampling)



(Courtesy of T.Schilcher/ PSI – CAS)

• Simplified block diagram of a down-converter :



Sample frequency:

$$f_s = \frac{N}{M} \cdot f_{IF} \quad N, M: \text{integers}$$

N samples in M IF periods

Phase advance:

$$\Delta\varphi = \omega_{IF} T_s = 2\pi \frac{T_s}{T_{IF}} = 2\pi \frac{M}{N}$$

$$I = \frac{2}{N} \cdot \sum_{i=0}^{N-1} y_i \cdot \sin(i \cdot \Delta\varphi)$$

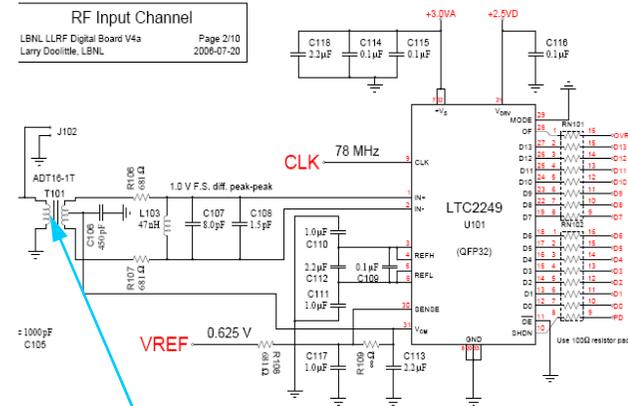
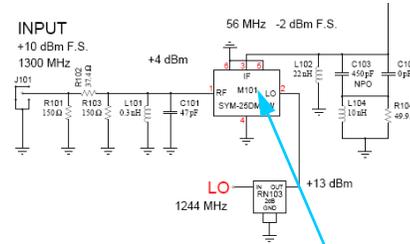
$$Q = \frac{2}{N} \cdot \sum_{i=0}^{N-1} y_i \cdot \cos(i \cdot \Delta\varphi)$$

LBNL: L. Doolittle, ORNL: Hengjie Ma, Mark Stuart Champion



ILC LLRF Eval Board

Input Channel:

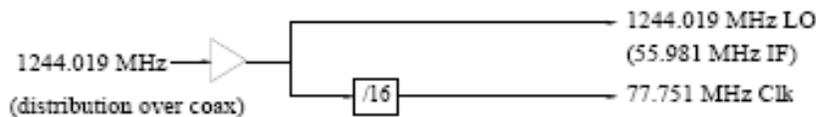


High IP3 Mixer!

Step-Up-Transformer

Properties :

- Controller Board including Mixer, ADC, FPGA, DAC
- 4 Input Channels with
 - Mixer SYM-25DMHW
 - High speed ADC (LTC2249 80MS/s)
- Clock can be derived from LO via AD9512:

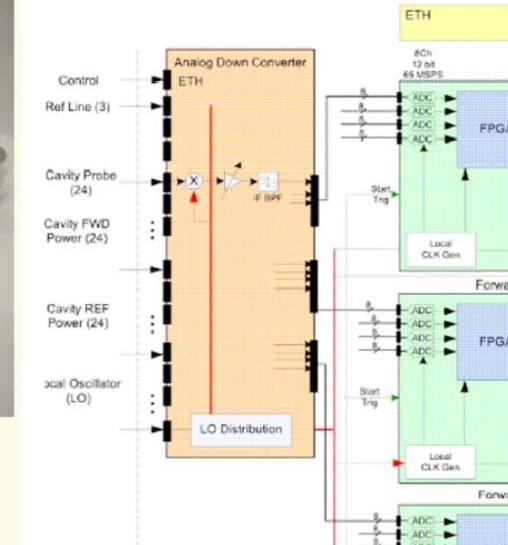
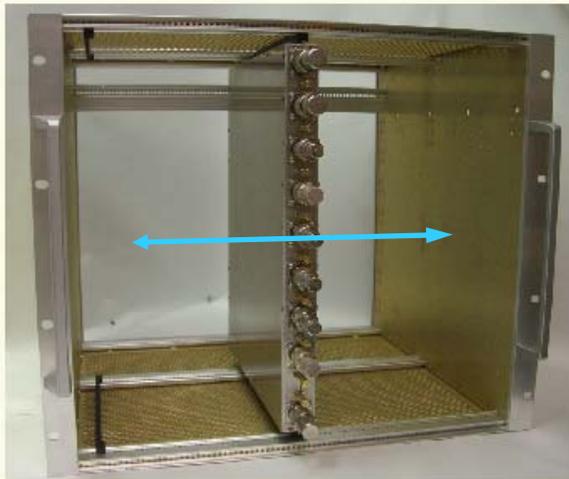
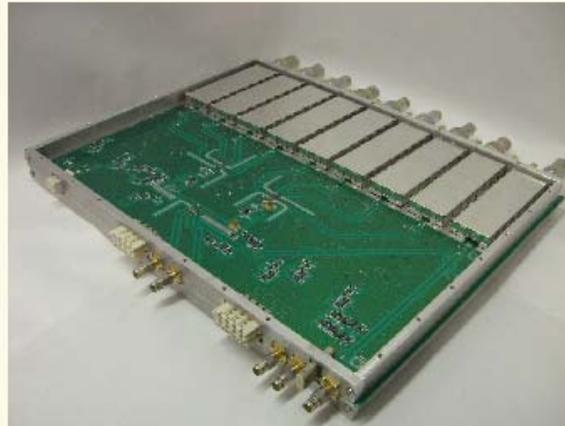


Project Status (May 07):

- 6 boards existing
- Problems with LO distribution
 - no up-/down-conversion

This 'Eval'-Board gave strong impulse to the LLRFcommunity!

Pictures of the Receiver

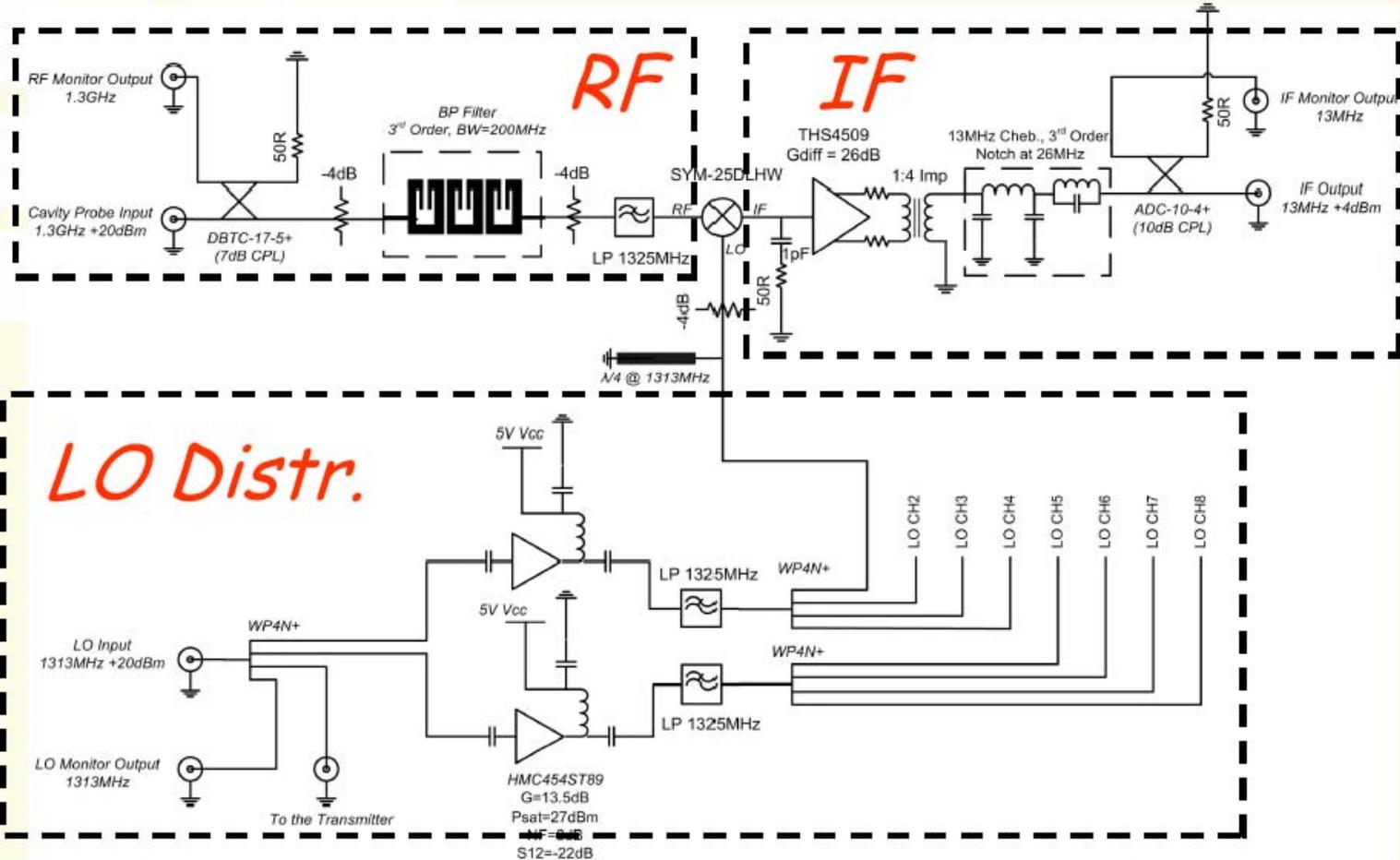


- Perfect packaging
- Scaleable for ,parallel' Detectors
- Clear analog digital separation

LLRF07

Courtesy of U.Mavric, B.Chase / FNAL

Schematic of the Rc



LLRF07

Fermilab



Courtesy of U.Mavric, B.Chase / FNAL

Main Parameters Table

<i>Parameter</i>	<i>Value</i>
Amplitude Noise	31dB (Input Noise Figure)
Residual Phase Noise	$1e-3^\circ$ (100kHz & Vec Sum)
Linearity	+35dBm (Input Pip3)
Temperature Sensitivity of Phase	???
Cross-Talk	71-90 dB (7 Ch. Connected)
Power Consumption	8W (1A@+6V/0.4A@-6V)
Number of Channels per board	8
Cost/Channel	150\$

Really good!

LLRF07

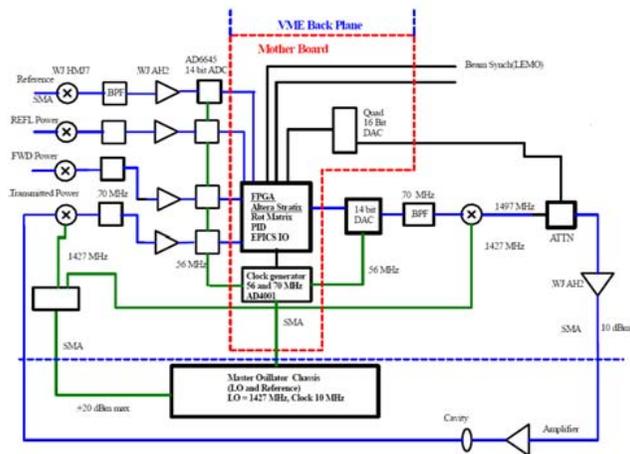
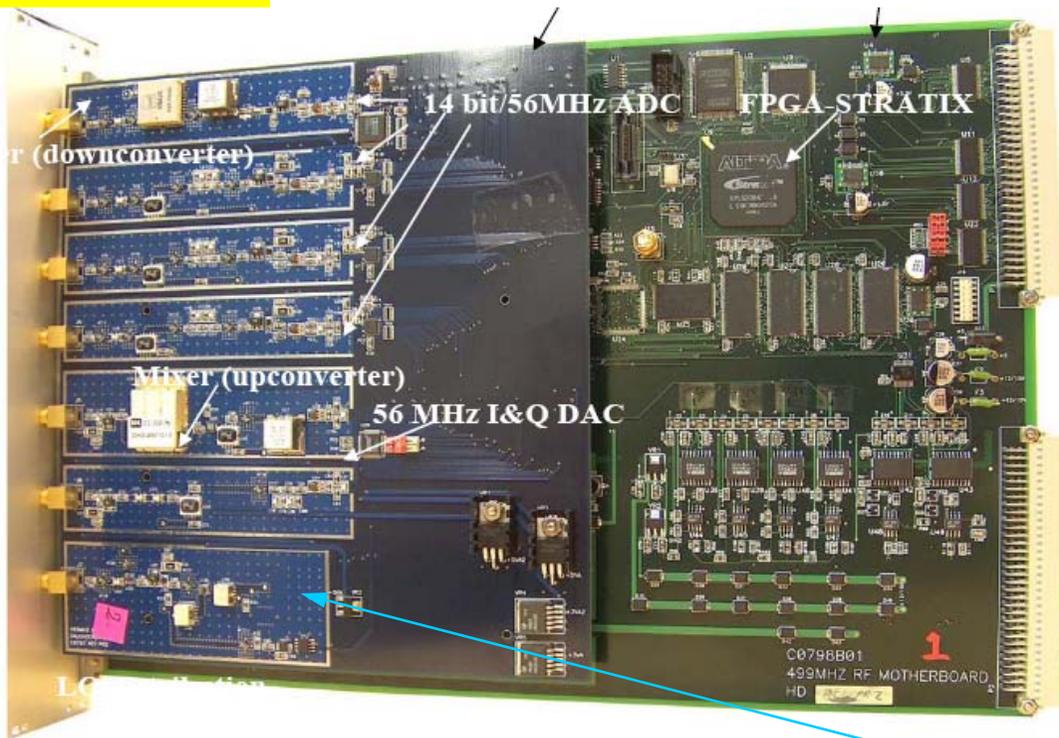


Fermilab



Courtesy of U.Mavric, B.Chase / FNAL

JLAB: C. Hovater



Receiver:

WJHMJ7 (high IP3) + AD6645 ADC

IF: 70MHz, Clk: 56MHz (AD4001)

2006: FPGA motherboard with special purpose daughterboard

Piggy-pack board down-converter!

• **Results :**

1497 MHz version has already received preliminary testing on a SC cavity:

- Phase: $\sim 0.3^\circ$ rms
 - Amplitude: $\sim 3 \times 10^{-4}$ rms
- (values: LINAC2006)

- Problem: one ADC per cavity → difficulties in board design
- Solution: Multi-IF scheme - two different IFs combined and then sampled

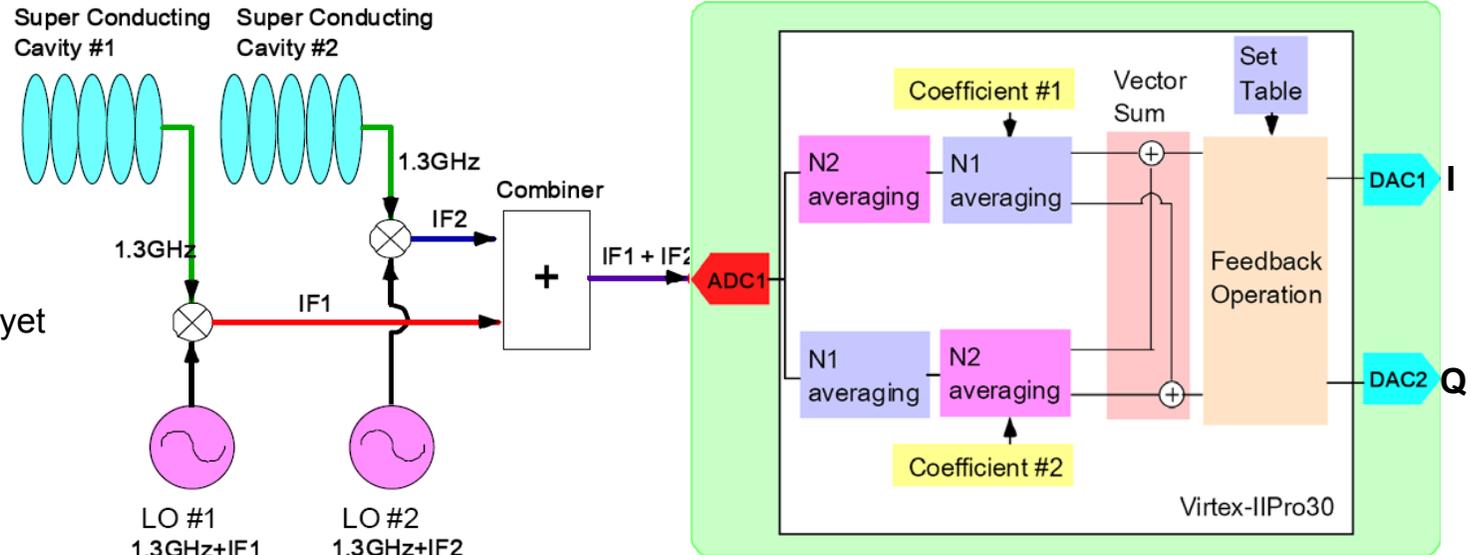
Test set-up:

SR = 40.625 MHz

IF₁ = 6.77 MHz

IF₂ = 10.16 MHz

No real downconverters yet
but FPGA based cavity
simulators



Advantages:

- number of ADCs reduced by half
- averaging reduces noise and jitter

Disadvantages:

- increased delay

Future plans:

- Three (or more) IFs
- Delay reduction → higher SR
- LO signal generation

KEK-STF phase 1 requirements:

$\Delta A = 0.3\%$

$\Delta\phi = 0.3^\circ$

Results_{RMS}:

$\Delta A = 0.11\%$

$\Delta\phi = 0.05^\circ$

Multichannel Packaging and Preprocessing

Multichannel Receiver frontend + fast ADC board for prototype testing : (DWC2.0, BAM1.0)

- Shielded subsections
 - Strong AGND to RF GND connections
 - Frontend mixer and ADC easily changeable
- (Applications:
Bunch-arrival-monitors,
Beam-position-monitors,
Beam-based feedback,
LLRF passive-active)

ADC:
(LT2207, 16Bit, 105MSPS)

Analog frontend:
(based on High IP3 Mixer HMC483)

IQ detection + fiber interface board : (ACB 2.0)

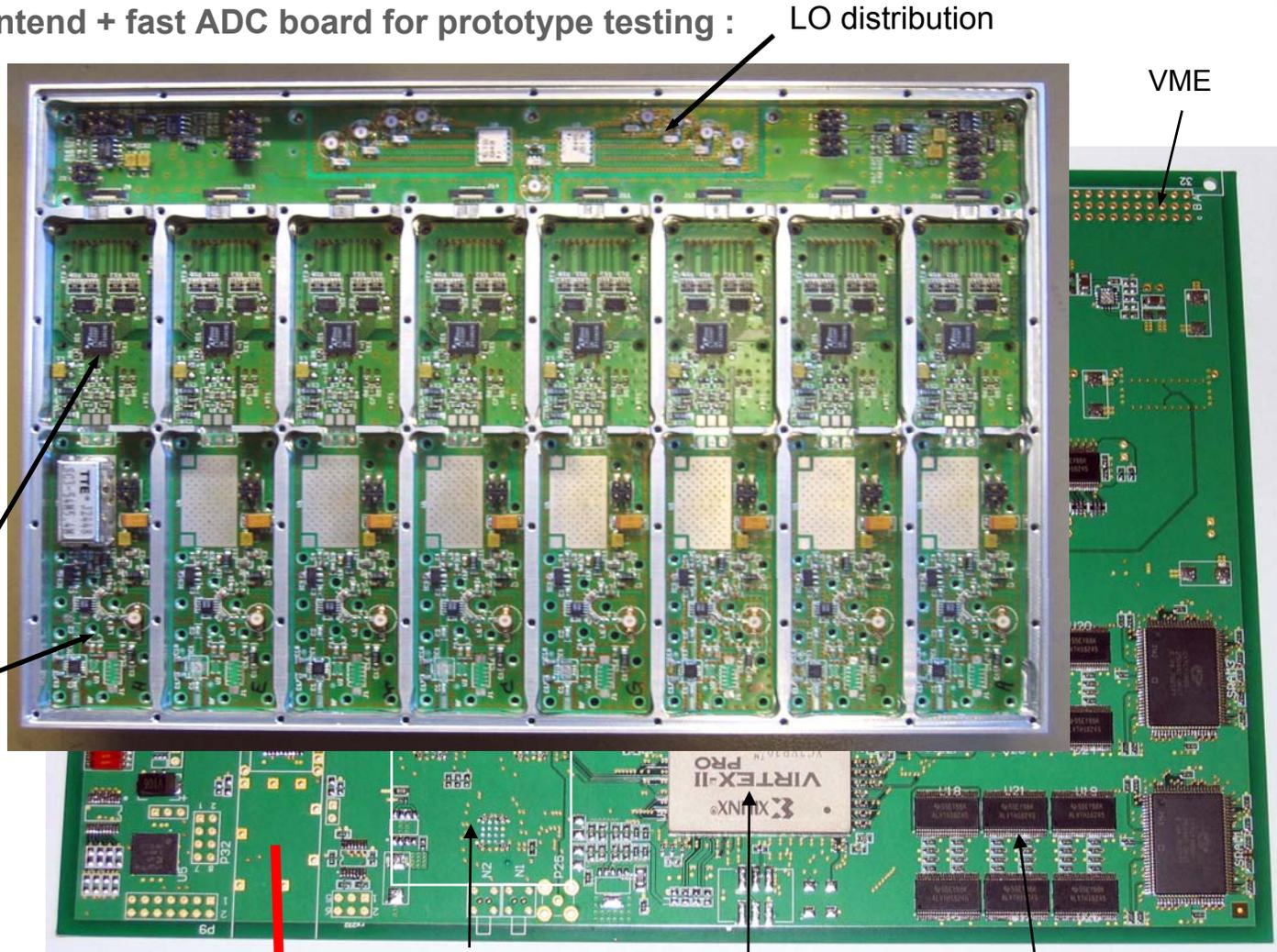
- 1Gbit/s Optolink,
- 1Gbit/s Ethernet
(Rocket IO Interface approx. 350ns latency)

Fiber interface to SIMCON DSP
(approx 400ns delay)

Clock shifting Unit:
(based on AD9510)

-FPGA pre-processing
(board 130ns latency)

- Macrobunch Buffer
(approx. 64MB)



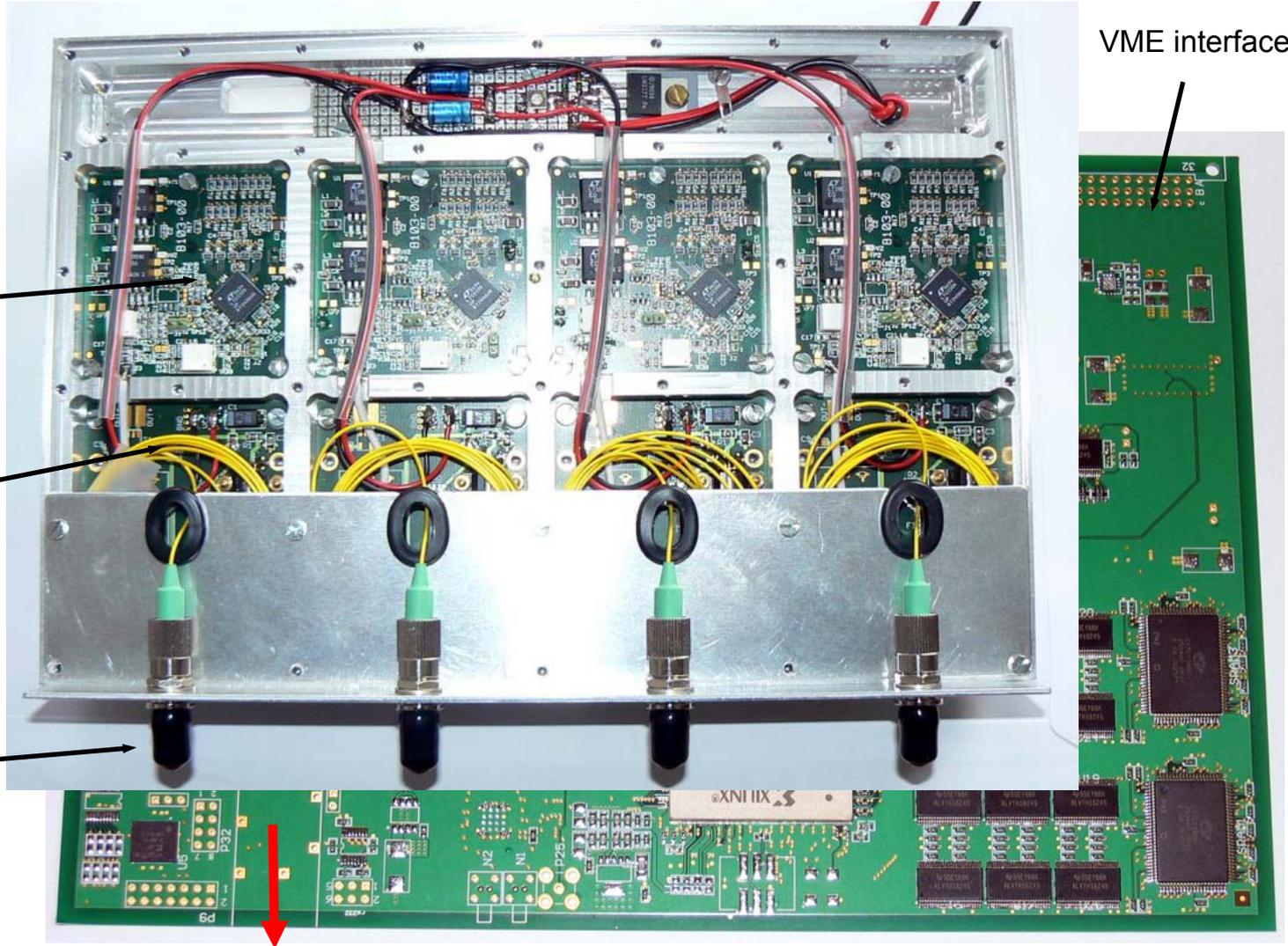
Other Applications :
Bunch-Arrival-Monitor
for a resolution $< 10\text{fs}$

16-Bit ADC,
130Mps

RF-frontend

Fiber Signal
Input

VME interface



Fiber interface
to SIMCON DSP

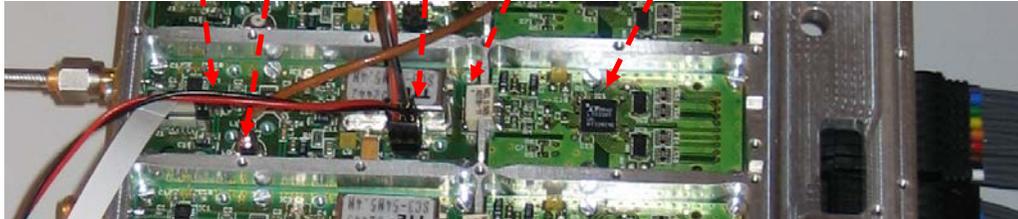
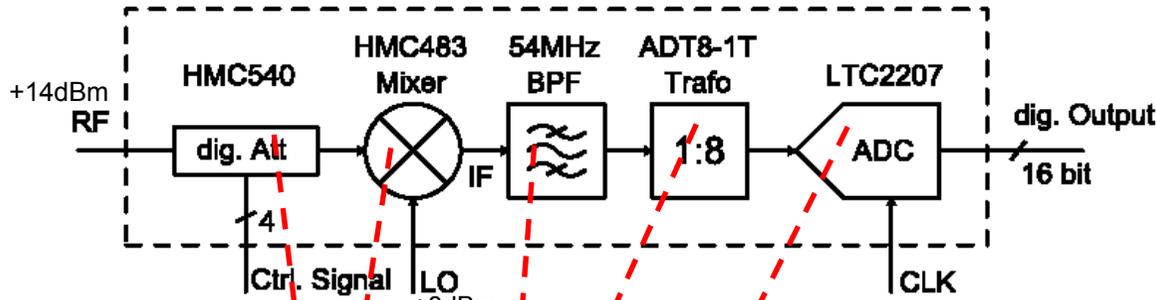
Digital motherboard (ACB 2.0):

- Provides Preprocessing and Fiber interface to controller

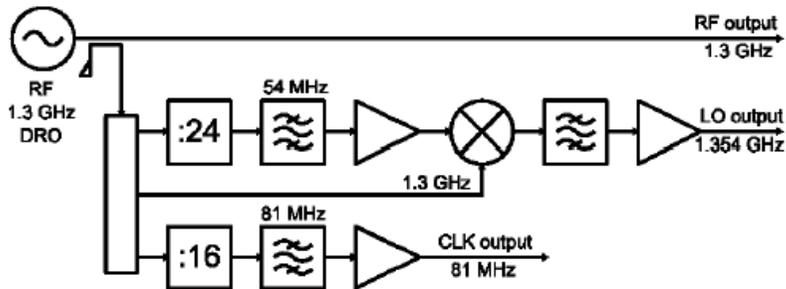
Single channel passive IF sampling down-converter

Laboratory performance :

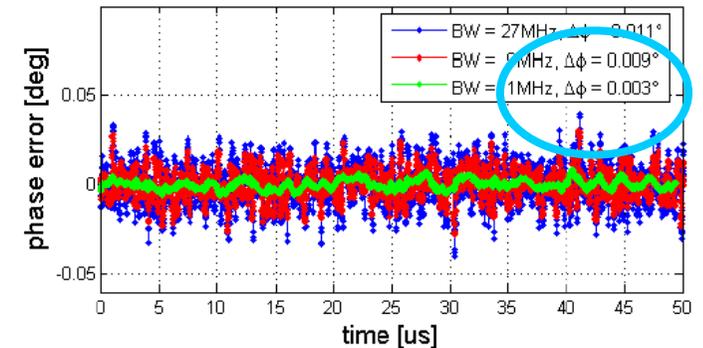
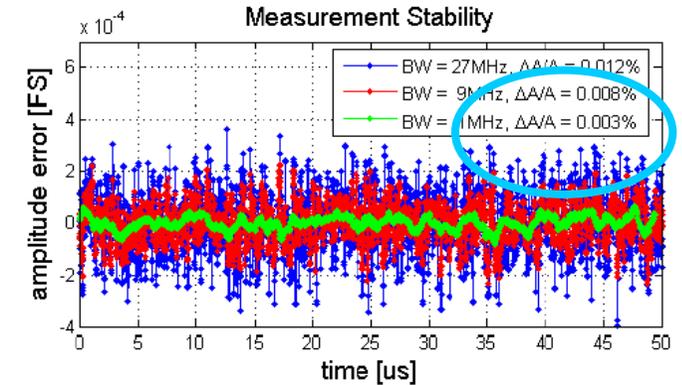
	Att.	Mixer	BPF	Trafo	ADC	System
NF [dB]	1	11	3	1	35	41
IIP3 [dBm]	48	36	35	35	/	36
G [dB]	-1	-11	-3	9	/	-6



LO and CLK Generation setup :



Shortterm stability :



Shortterm stability (1MHz Bandwidth) :

$$\theta_A = 3E-3, \theta_P = 3m^\circ$$

Drift stability :

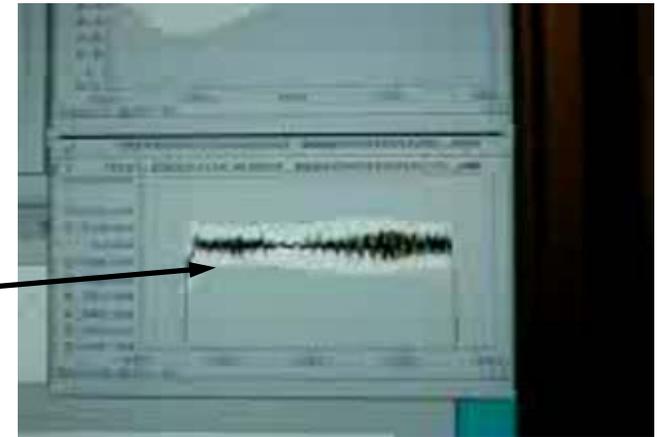
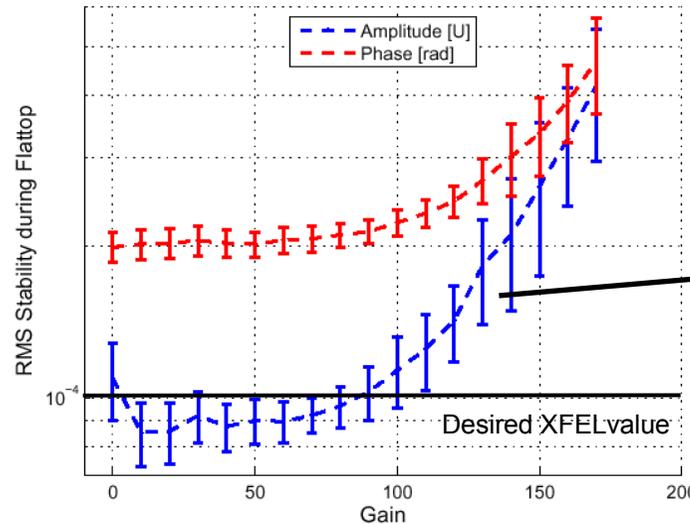
$$\theta_A = 3e-3/^\circ C, \theta_P = 0.2^\circ/^\circ C$$

Receiver performance at FLASH

- FLASH injector :

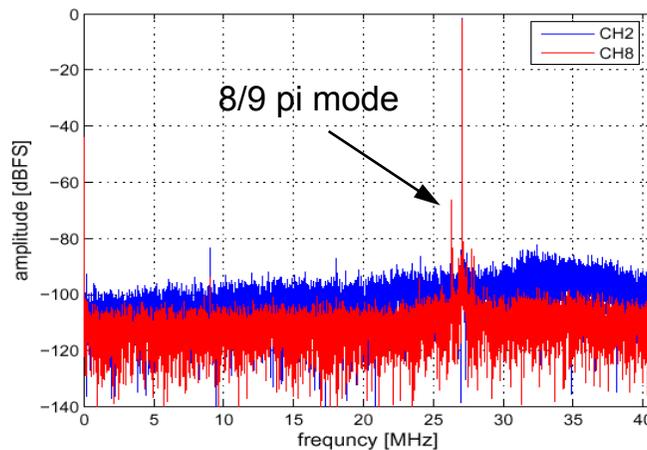


- Vectorsum stability with closed control loop at ACC1:



Instability caused by 8/9pi mode

Down-converter biased by Cavity pickup :



	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
$\Delta A/A$ [10^{-4}]	3.8	5.8	5.1	4.1	2.8	4.1	2.1	3.6
$\Delta \varphi$ [deg]	0.028	0.038	0.035	0.033	0.025	0.032	0.022	0.032
$\Delta A/A$ [10^{-4}]	2.1	2.5	1.9	1.6	1.0	1.5	0.9	1.5
$\Delta \varphi$ [deg]	0.016	0.019	0.018	0.021	0.016	0.020	0.015	0.019

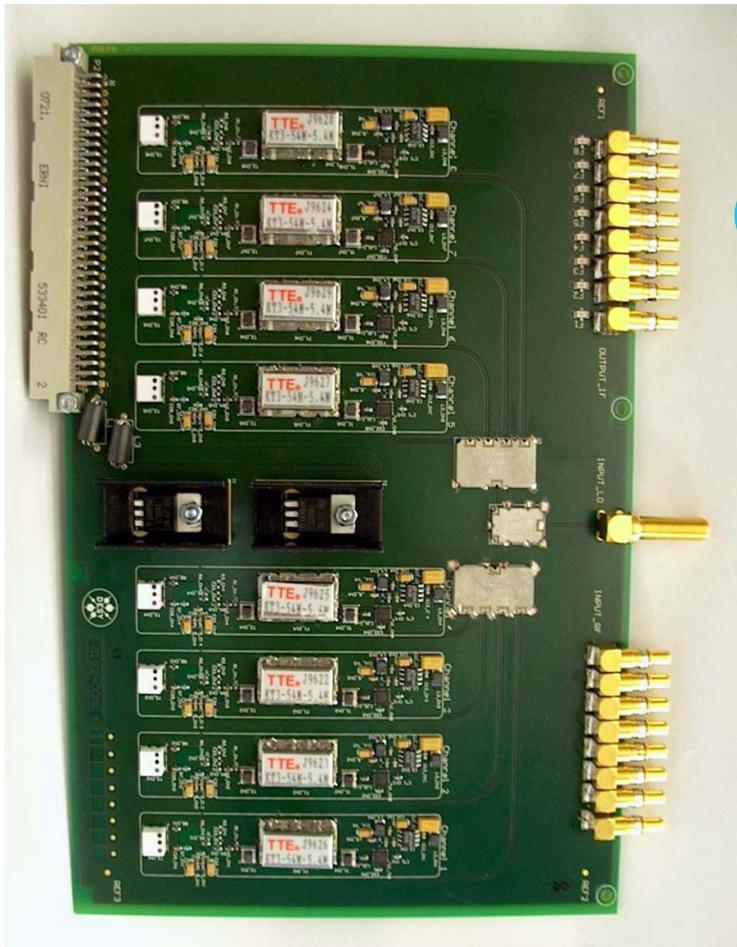
- Down-converter fulfill XFEL specs
- Spurious signals are below 80dBc
- Cavity 8/9pi mode clearly measurable

Single channel receiver performance at FLASH

- FLASH injector :

- Biased by MO reference :

- Shortterm stability 800us (bunch-to-bunch):



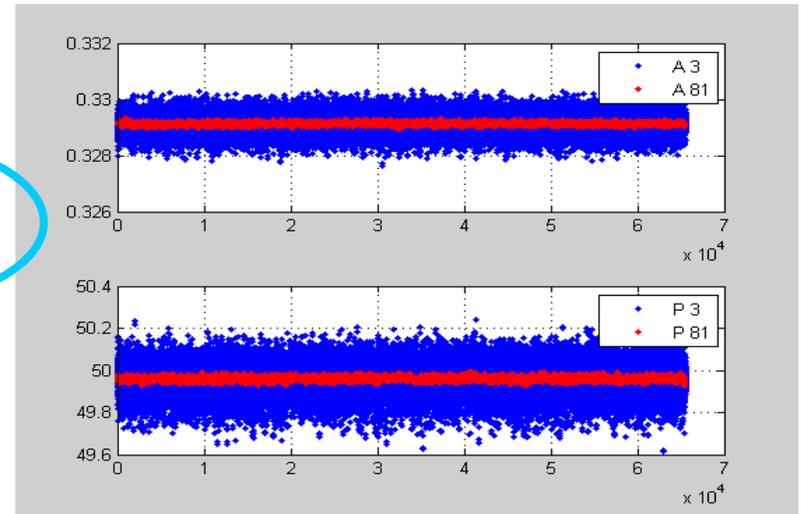
BW=27MHz
 BW=1MHz

$\Delta A_3 = 9.3377e-4$
 $\Delta A_{81} = 1.4942e-4$
 $\Delta P_3 = 0.0654 \text{ deg}$
 $\Delta P_{81} = 0.0092 \text{ deg}$

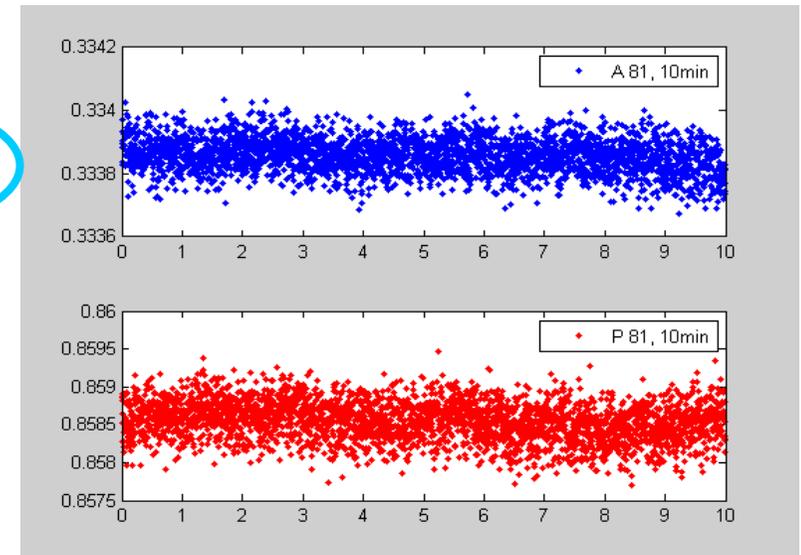
$$: \sqrt{8}$$

BW=1MHz
 BW=1MHz

$\Delta A = 1.6263e-004$
 $\Delta P = 0.0147 \text{ deg}$



- Midterm stability 10min (pulse-to-pulse):



- 8x LT5527(Gilber-mixer), x6 OPV-Amplification

+ SIMCON DSP (14-Bit ADC)

81 samples over 1 us

→ 1 IQ value

→ ~5 Hz through 10 minutes

Single channel receiver performance at FLASH

- FLASH injector :
- Single channel receiver performance at a CW IF :
- Incl. LO-Generation phase noise

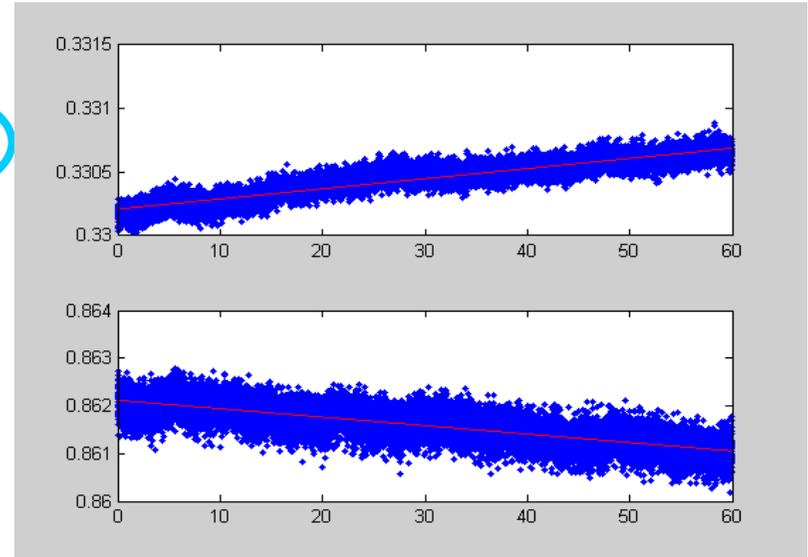
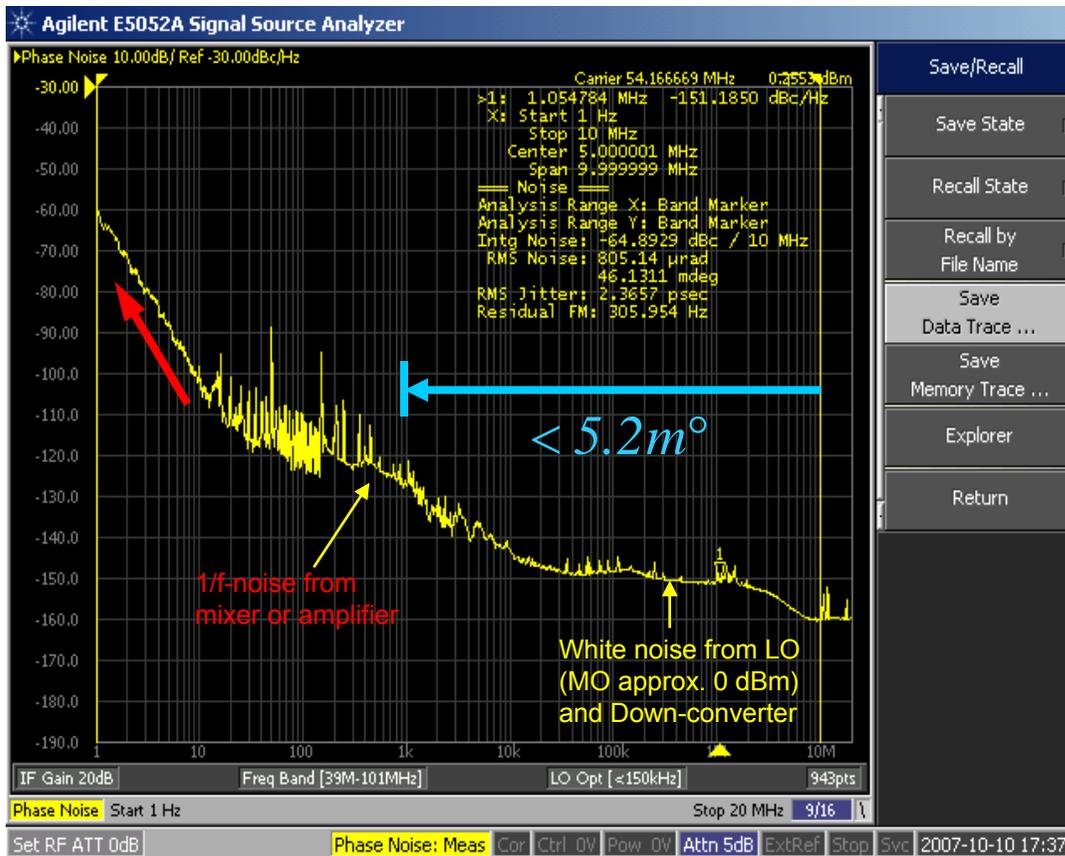
Biased by MO reference :

BW=1MHz

$\Delta A = 1.8136e-004$

$\Delta P = 0.0147 \text{ deg}$

- Long-term stability 1 hour (drifts):



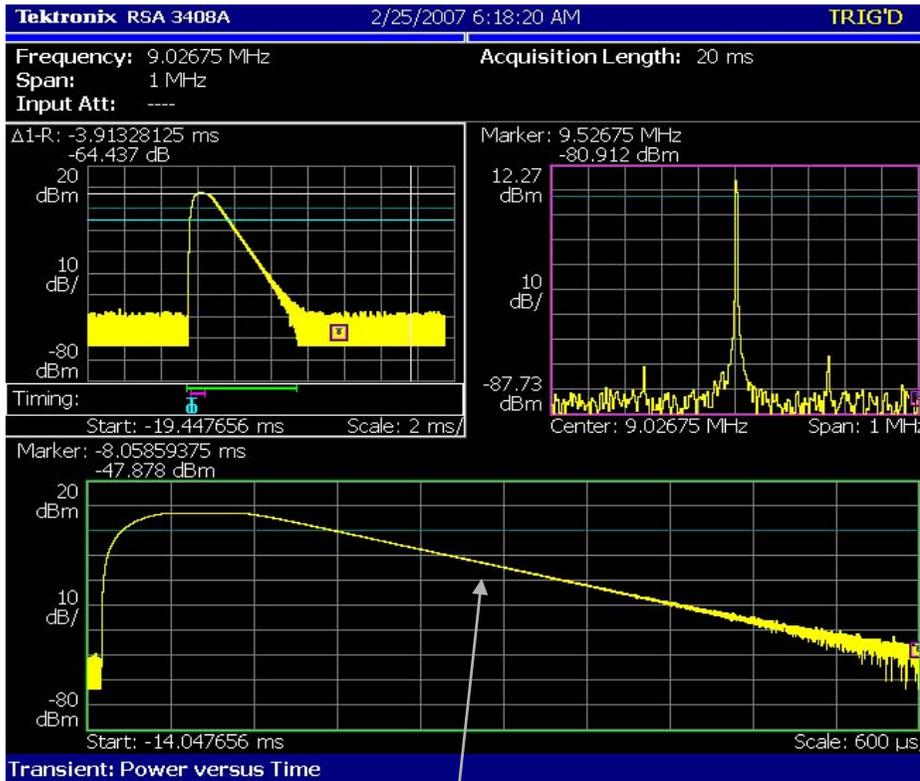
Amplitude and phase stability measured after subtracting slope

- Analog Receiver has 0.0052 deg
- IF[9,54MHz] works also with a lowpass
- Apply 1/f-noise reduction methods
- Easy investigation and servicing of LO and IF signals using a CW modulation
- Drift calibration >10Hz is needed proposed by L.Doolittle or Beam-based feedbacks

- Compensate drifts from down-converter LO, CLK Generation
- Separation from Synchronization System ●

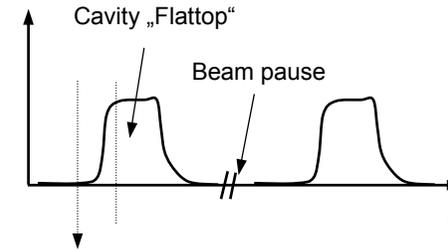


● Linearization using the probe cavity decay:



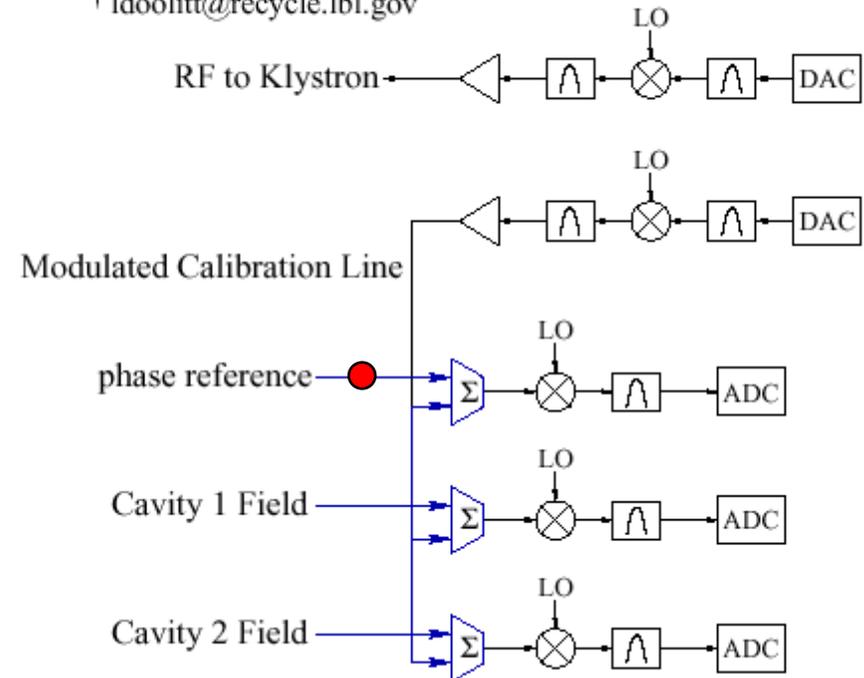
Quit good exponential decay
 Possible hardware linearization of DWC's

● Off beam phase calibration :

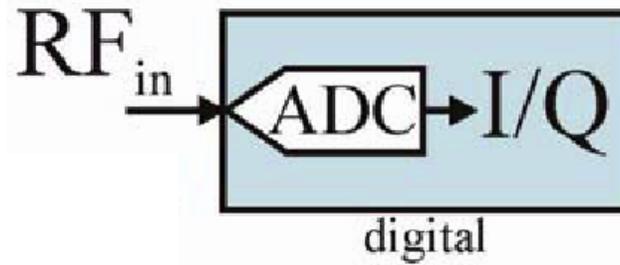


Calibration of the down-converter phase using a local rf-reference.

Lawrence Doolittle[†], LBNL, Berkeley, California
[†] ldoolitt@recycle.lbl.gov



Direct sampling



(Courtesy of T.Schilcher/ PSI – CAS)

What's the time ?

Direct Sampling of RF signals

• Key features :

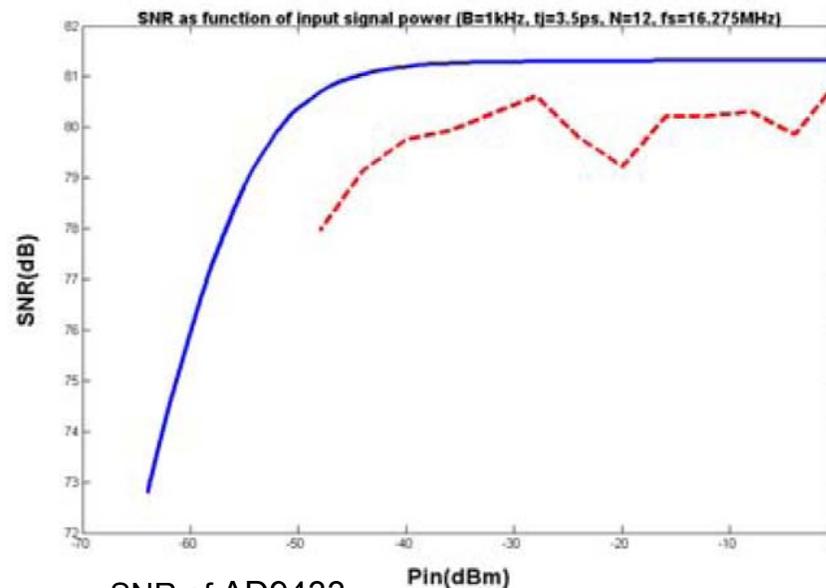
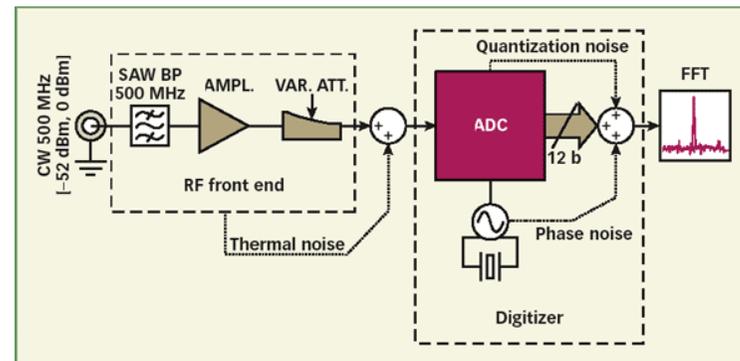
- simplifies RF frontend (no downconversion)
- amplifier & attenuator to match to the input range of the ADC
- undersampling inevitable
→ $BW < f_s/2$

• SNR :

- amplifier noise
- ADC quantization noise
- clock jitter

• Linearity :

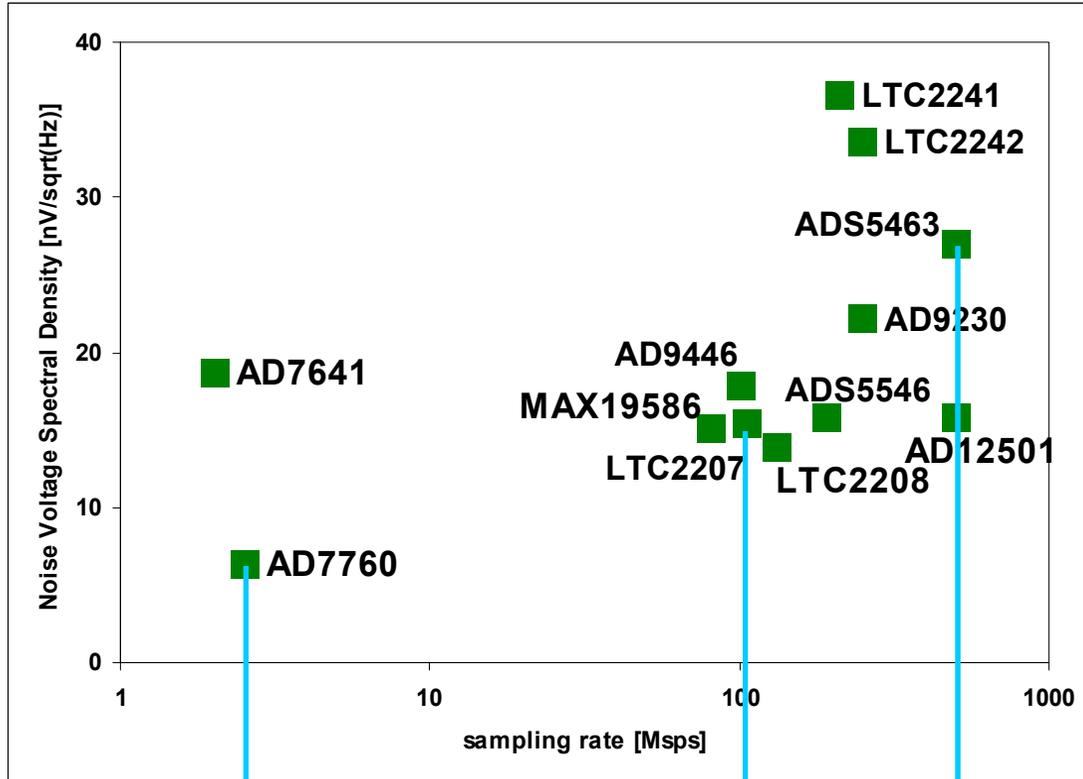
- amplifier linearity (compression)
- ADC linearity



SNR of AD9433
calculated (solid) & measured (dashed)
 $f_{in} = 200\text{MHz}$, $f_s = 16.3\text{MHz}$

Courtesy of U.Mavric / FNAL

- ADC equivalent noise spectral density :



Baseband or IF Detection

IF Sampling

Direct Sampling

$$e_n = \frac{V_{FS,pp}}{\sqrt{8}} 10^{\frac{SNR(f_s, \epsilon)}{20}} \sqrt{\frac{2}{f_s}}$$

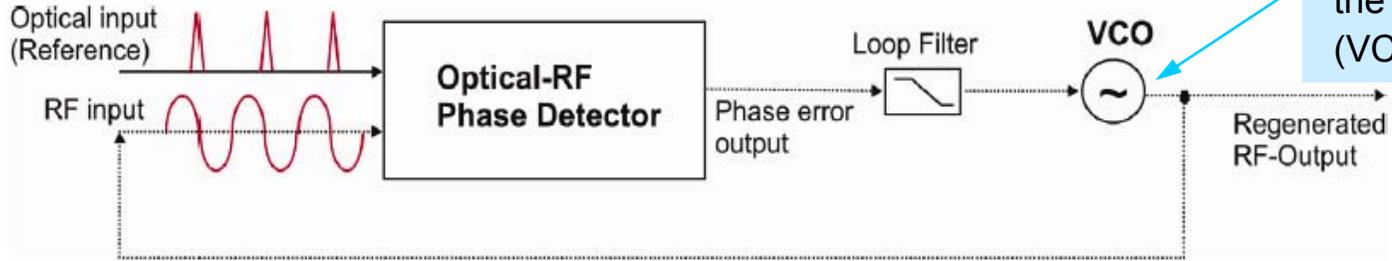
Typ	Bits	$f_{s,max}$ [MSPS]	SNR [dBFS] 70 MHz	SFDR [dBc] 70 MHz	V_{FS} [V _{pp}]	t_j [fs]
LTC2207	16	105	77.5	90	2.25	80
LTC2208	16	130	77.5	90	2.25	70
AD6645	14	80	73.5	87	2.2	100
AD9461	16	130	77	84	3.4	60
AD9446	16	100	79	89	3.2	60
ADS5546	14	190	73.5	87	2.0	150



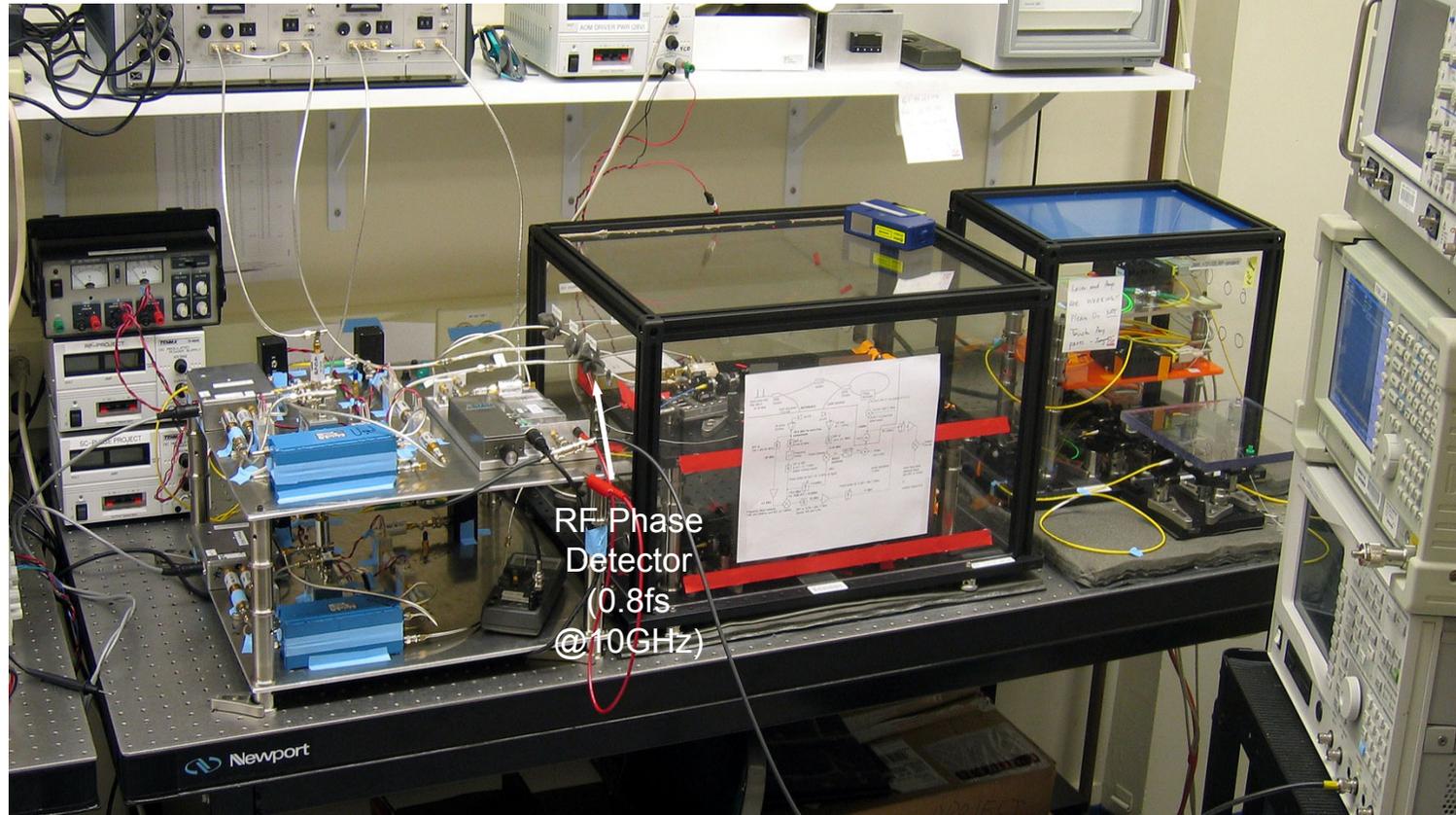
A lot of available ADCs have roughly the same performance.

Optical to RF conversion – sagnac loop

- Phase-locked loop (PLL) :

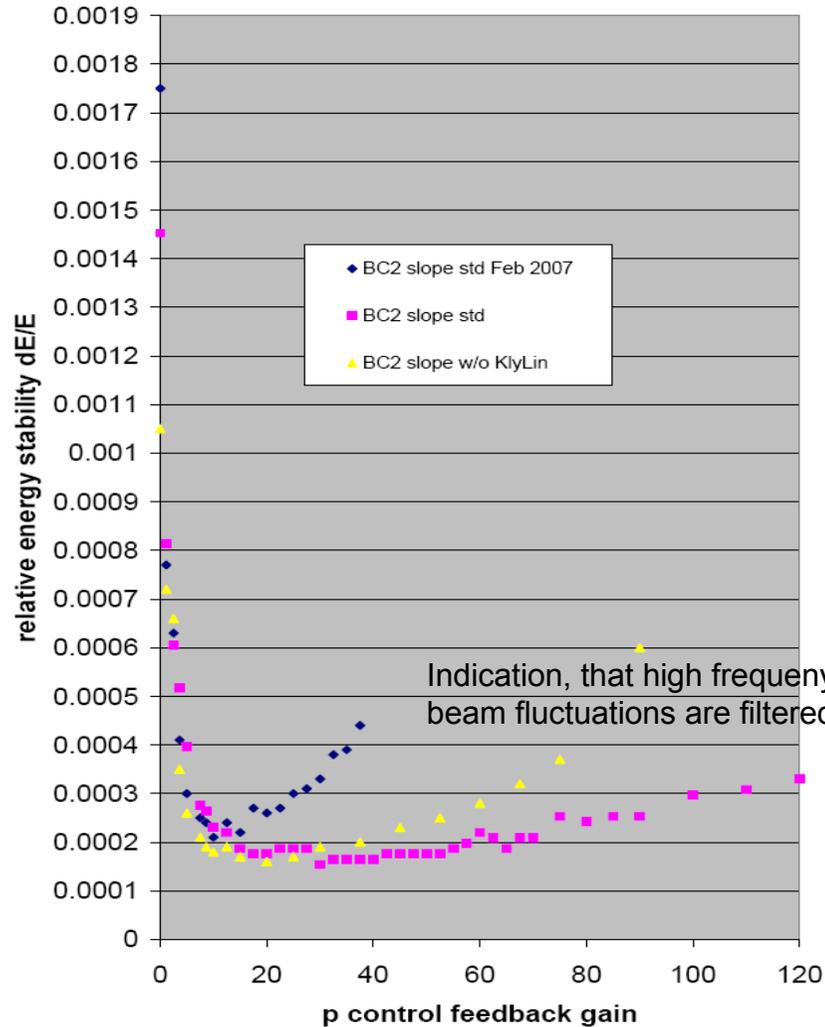


timing jitter between two VCOs locked via sagnac loop:
(10 Hz – 10 MHz):
12.8 fs @ 10 GHz
(drifts):
<50fs

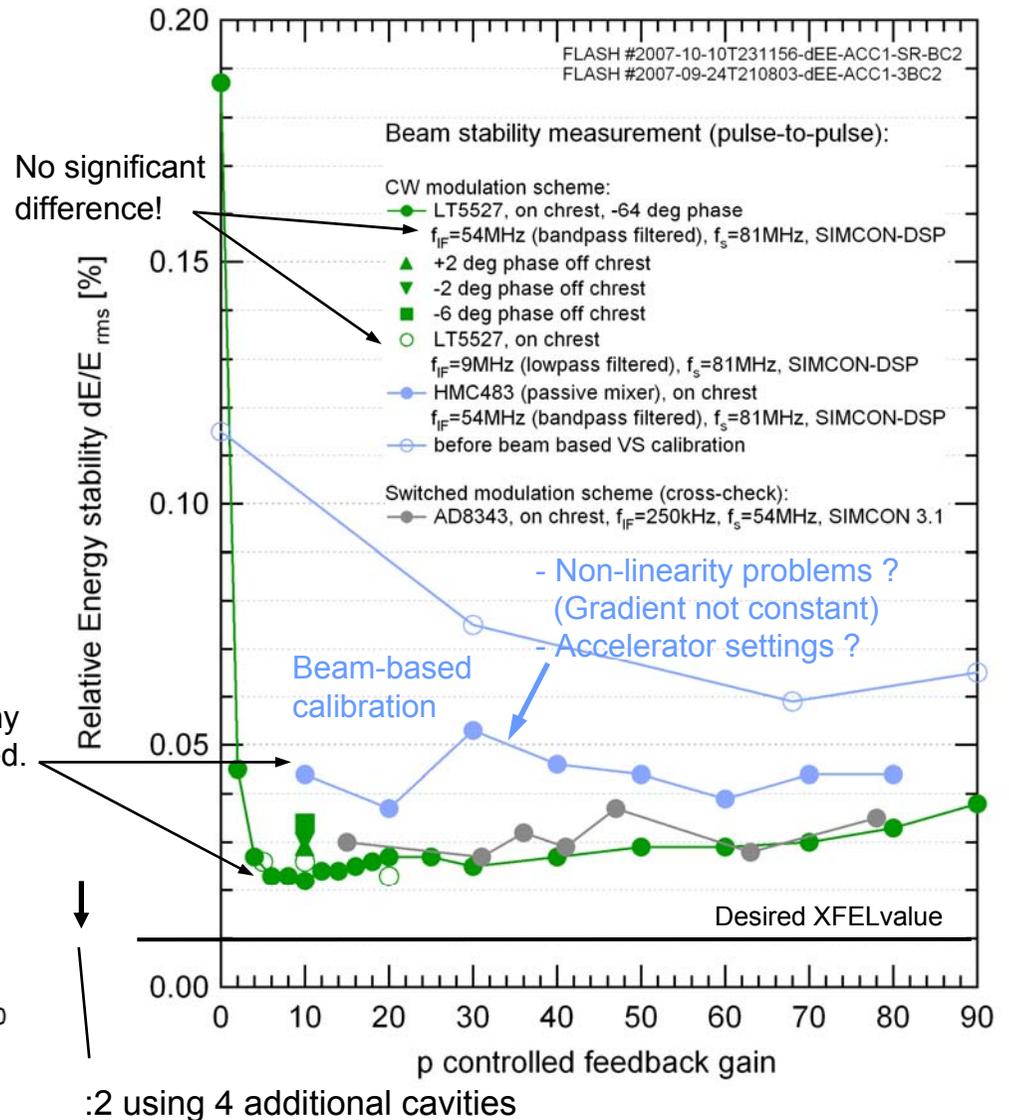


Beam stability measurements

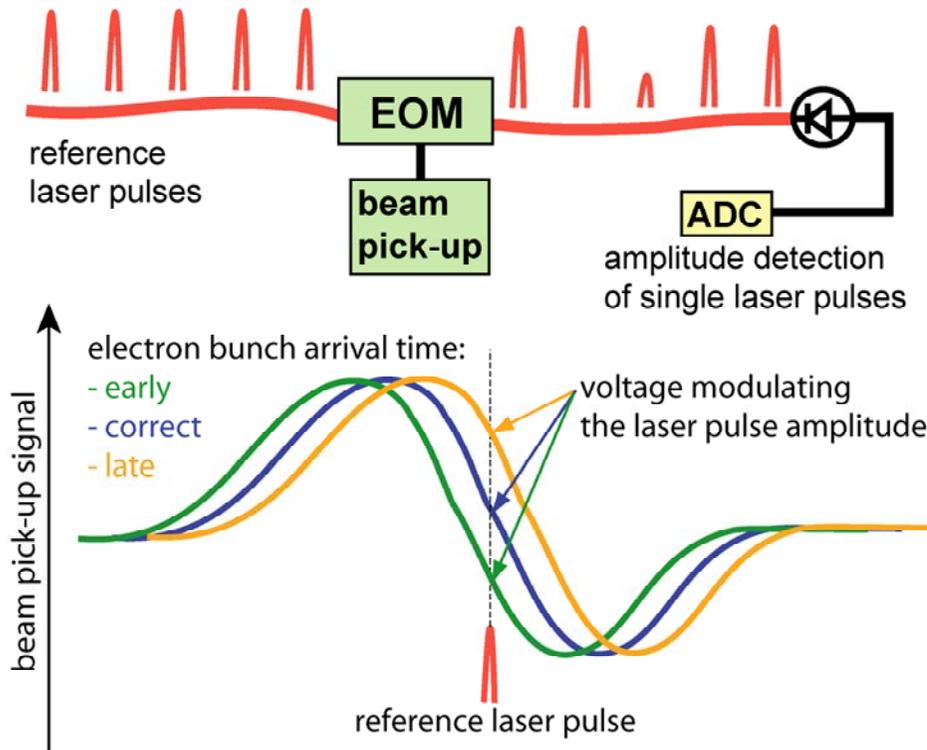
• IQ sampling down-converter (250kHz):



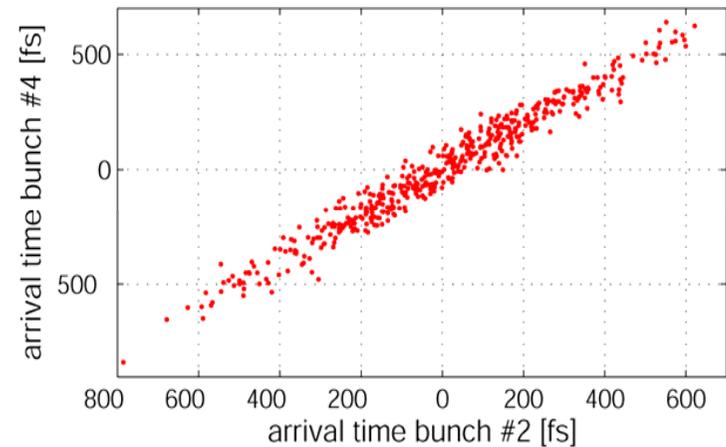
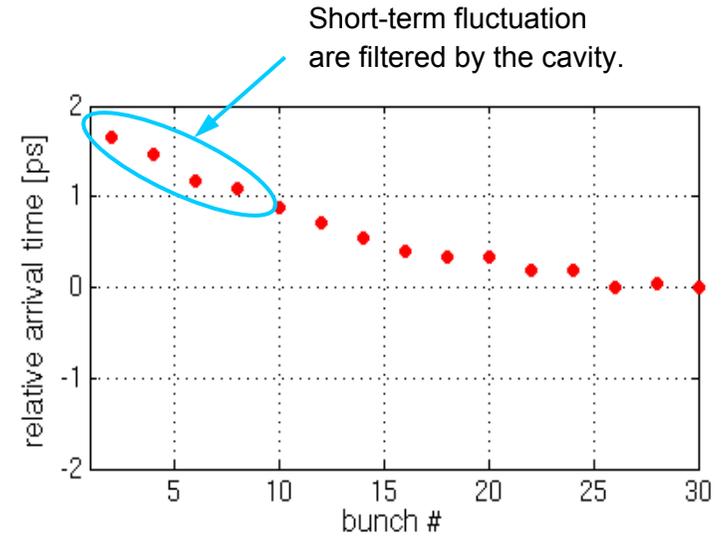
• IF sampling down-converters (9,54MHz):



● **Bunch-Arrival Monitor :**



- Single bunch resolution better 30fs
- Synchronization problems



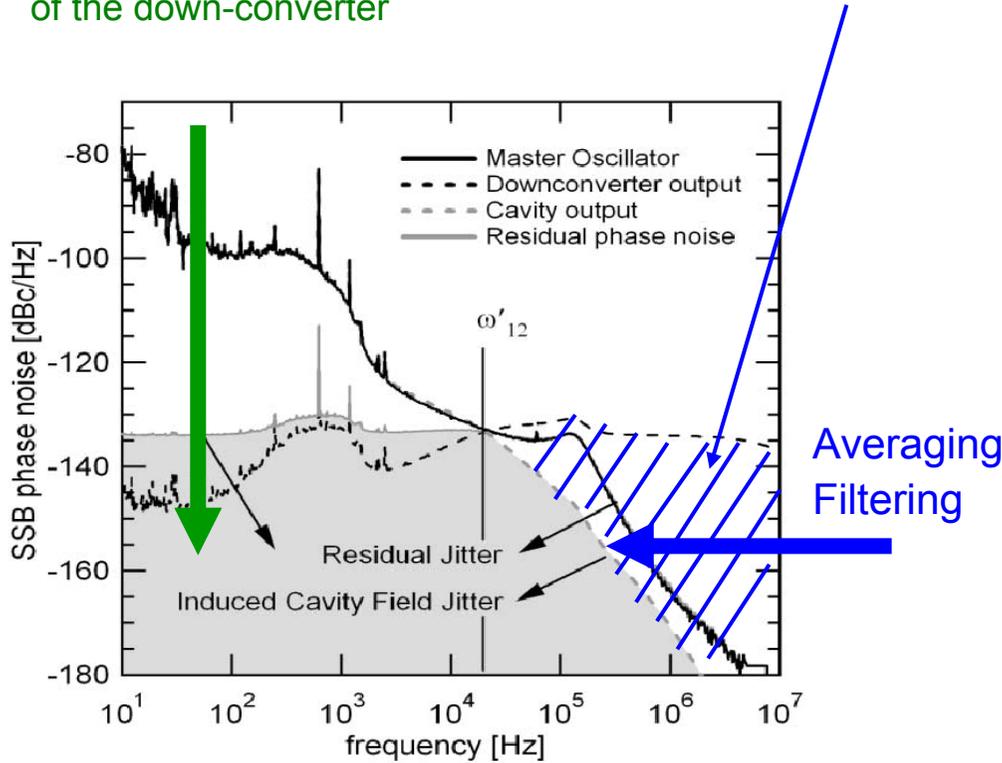
Courtesy of F.Loehl / DESY

„Beam performance“:

- Increase SNR by
 - Increasing input power
 - Decreasing noise spectra density of the down-converter

„Display property for the operator“:

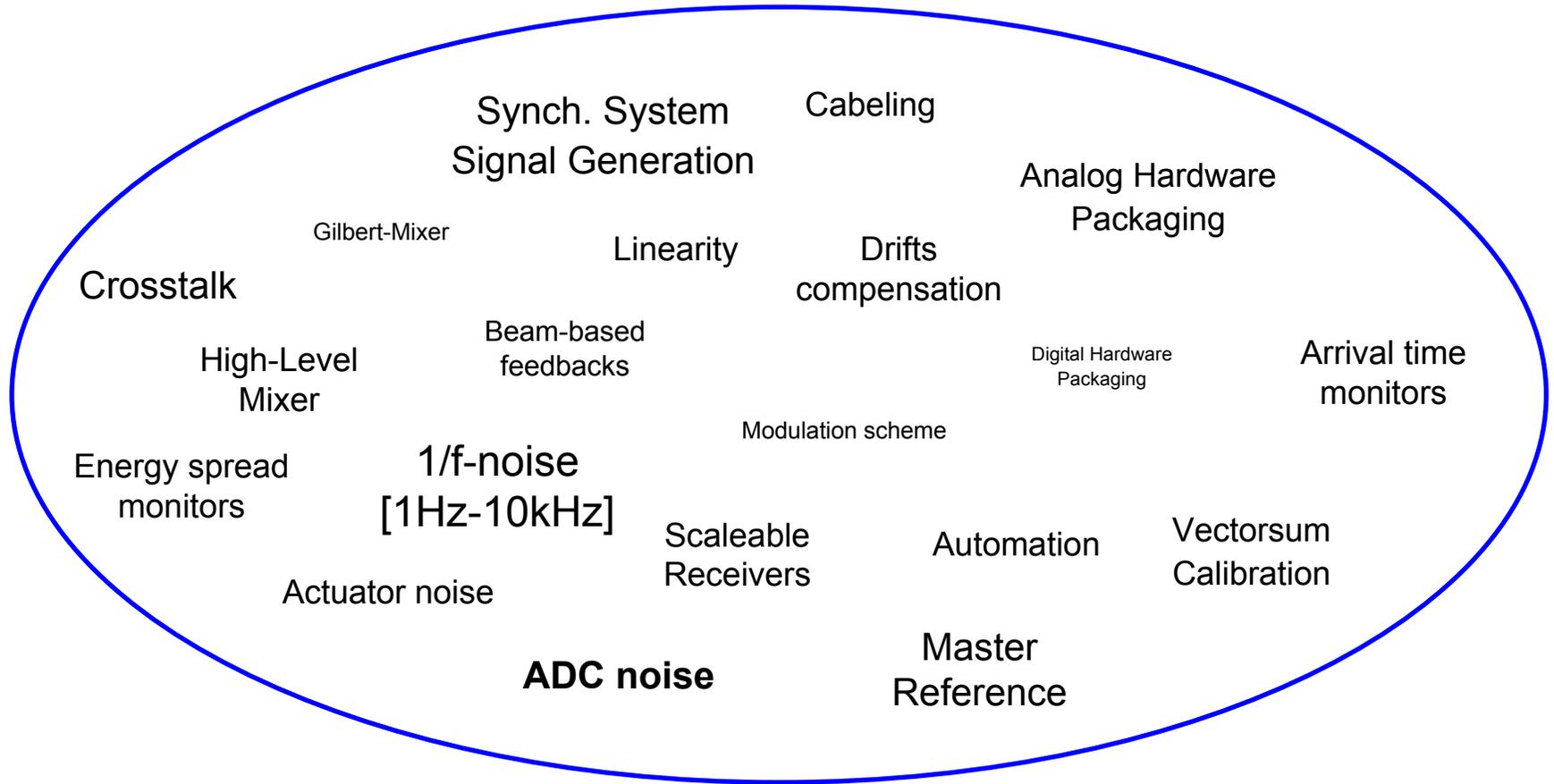
Noise appears at the DWC output but not on the cavity field!



← Effective noise bandwidth for the beam jitter induced by the LLRF



- Bunch-to-Bunch, Pulse-to-Pulse energy spread and arrival time monitors
- Automated beam-based calibration using a pilot macrobunch -> Optimization of fluctuations (for multi-cavity regulation)
- Passive High IP3 mixers
- 1/f-noise reduction methods
- Drift calibration (L.Doolittle)
- ADC limitation -> Multiple IF (KEK) -> bypass the ADC/P/DAC
- Parallel detectors -> scaleable packaging



What is most important for a beam stability significantly lower than 0.01% ?

Summary & Outlook

- All kind of different packaged multi-channel down-converter are available from the labs worldwide.
- The amplitude beam stability requirements for FLASH are nearly fulfilled:
0.016% using the IQ sampling scheme operating at 250kHz and
0.022% using the IF sampling scheme operating at 9MHz and 54MHz
- $1/f$ -noise, spurious (low frequency range) and IF amplification * (high frequency) are the main reason for the pulse-to-pulse beam jitter.
- A multi-channel down-converter from FNAL based on the IF sampling scheme is presented with excellent 1m deg. performance (proved in laboratory in the range [10Hz,100kHz]).
- An automated beam-based vectorsum calibration or optimization around minimum fluctuation using a pilot macro-bunch is needed.
Will clarify the question: How much linearity is really needed ? (Vary RF att. & post amp)
- Its worth switching to the IF sampling scheme, because of improved „vector sum display“ and powerful error diagnostic at the IF port.
- The performance of the drift calibration must be shown **AsSoonAsPossible!**

low noise...->...high linearity... -> ...low drift... -> ... absolute accuracy

Thanks for your attention!

* Linearity requirement for multi-cell cavity structures