ESECON
14 channel LLRF controller

LLRF Workshop 2007 Knoxville, TN

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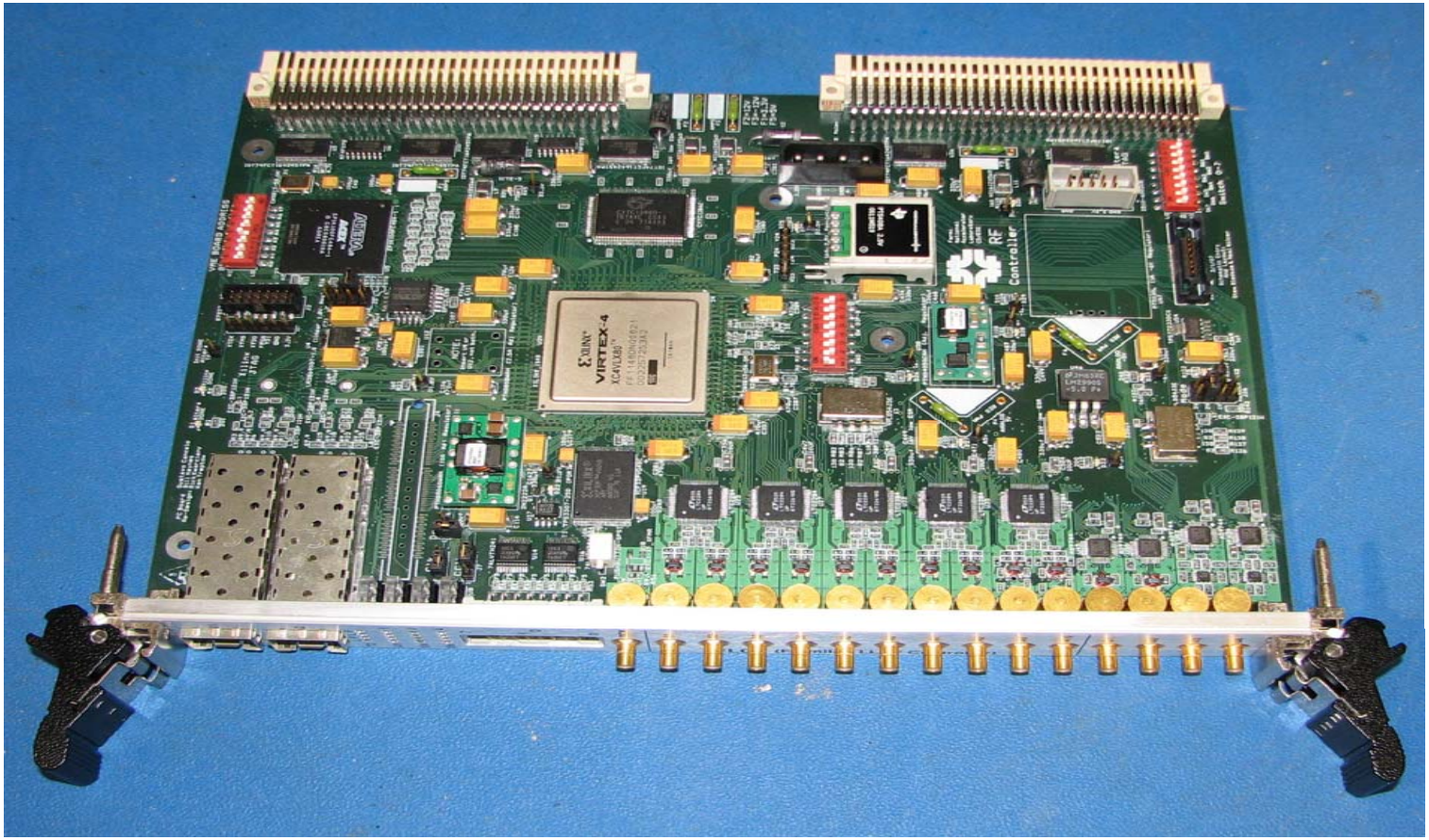
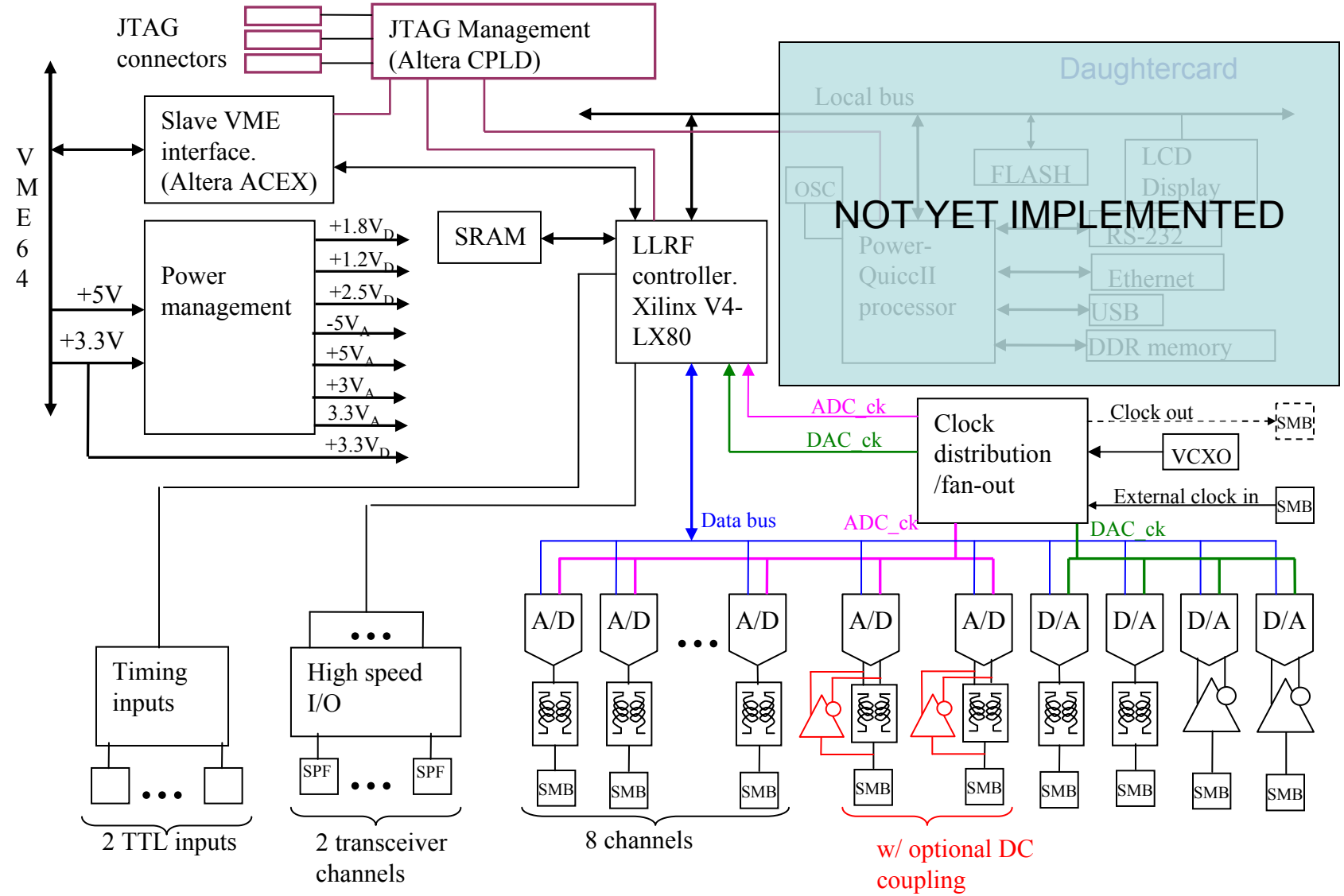
ESECON: 10 channel LLRF controller



The goal was to have a FNAL controller **functionally** compatible with DESY's Simcon3.1 to support LLRF systems at FNAL such as the A0 photoinjector, CCII, HTS and the NML cryomodules.
Other goals: minimize the noise and lower the power consumption across the board.

1st production of 6 boards completed in July 07 (no blue wires).
2nd production of 10 boards scheduled for early 08.

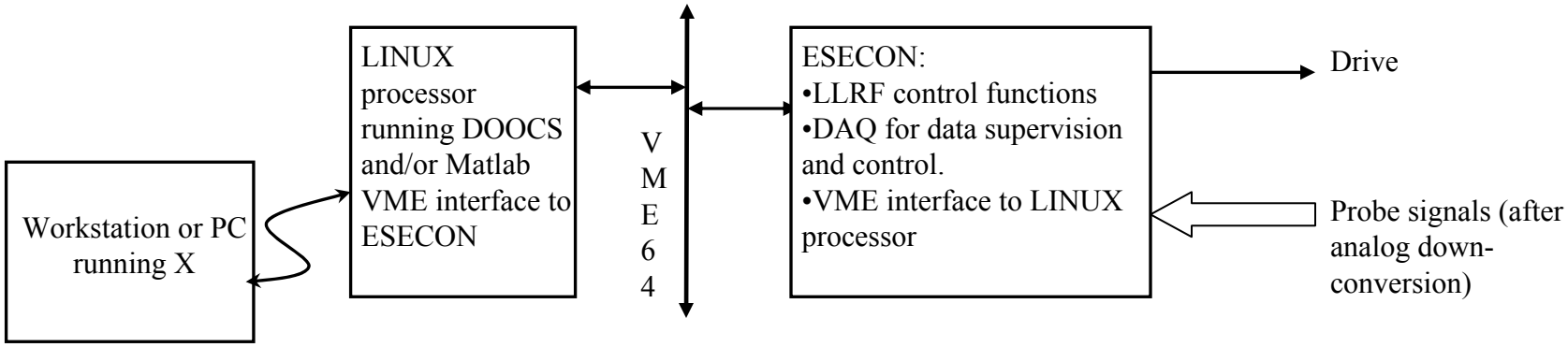
Controller block diagram



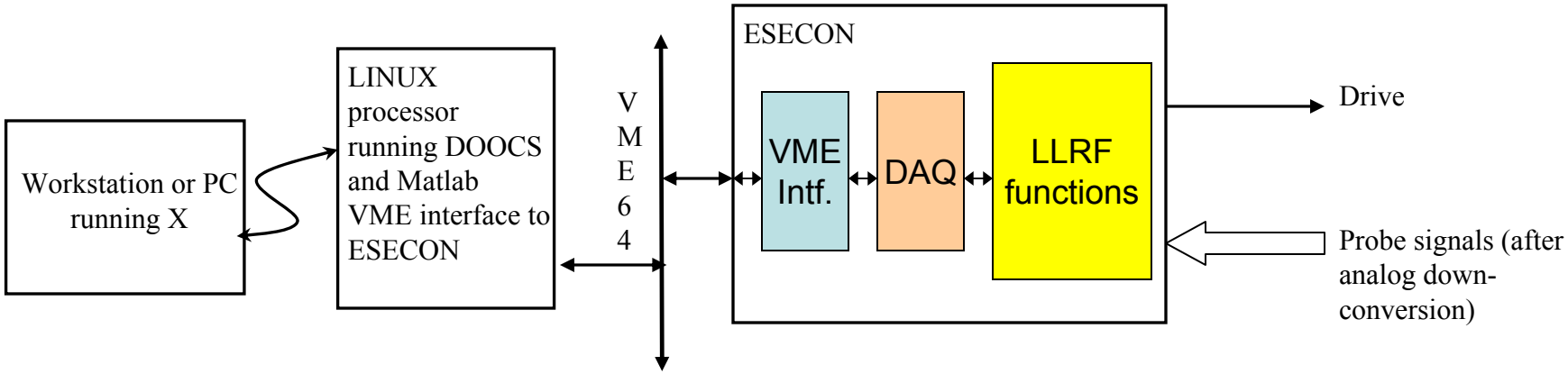
Some few specifications

- 10, 14-bit ADC channels,
  - Linear Technologies LTC2285: 105Ms/s, 640MHz Bandwidth. Low power 750mW/channel.
  - Input dynamic range ±1 volt, AC coupling, DC coupling available on two channels.
- 4, 14-bit 4 DAC channels,
  - Analog Devices AD9744, dynamic range ±1 volt.
  - Two AC coupled channels and two DC coupled channels.
- VME64 slave interface.
- Quiet power supplies with a mix of switched and linear.
- Tunable IF DDC with 0.012Hz resolution.
- Matlab and DOOCS software interface.
- DSP and control functions implemented in firmware (Xilinx Virtex4 FPGA).

ESECON functionality



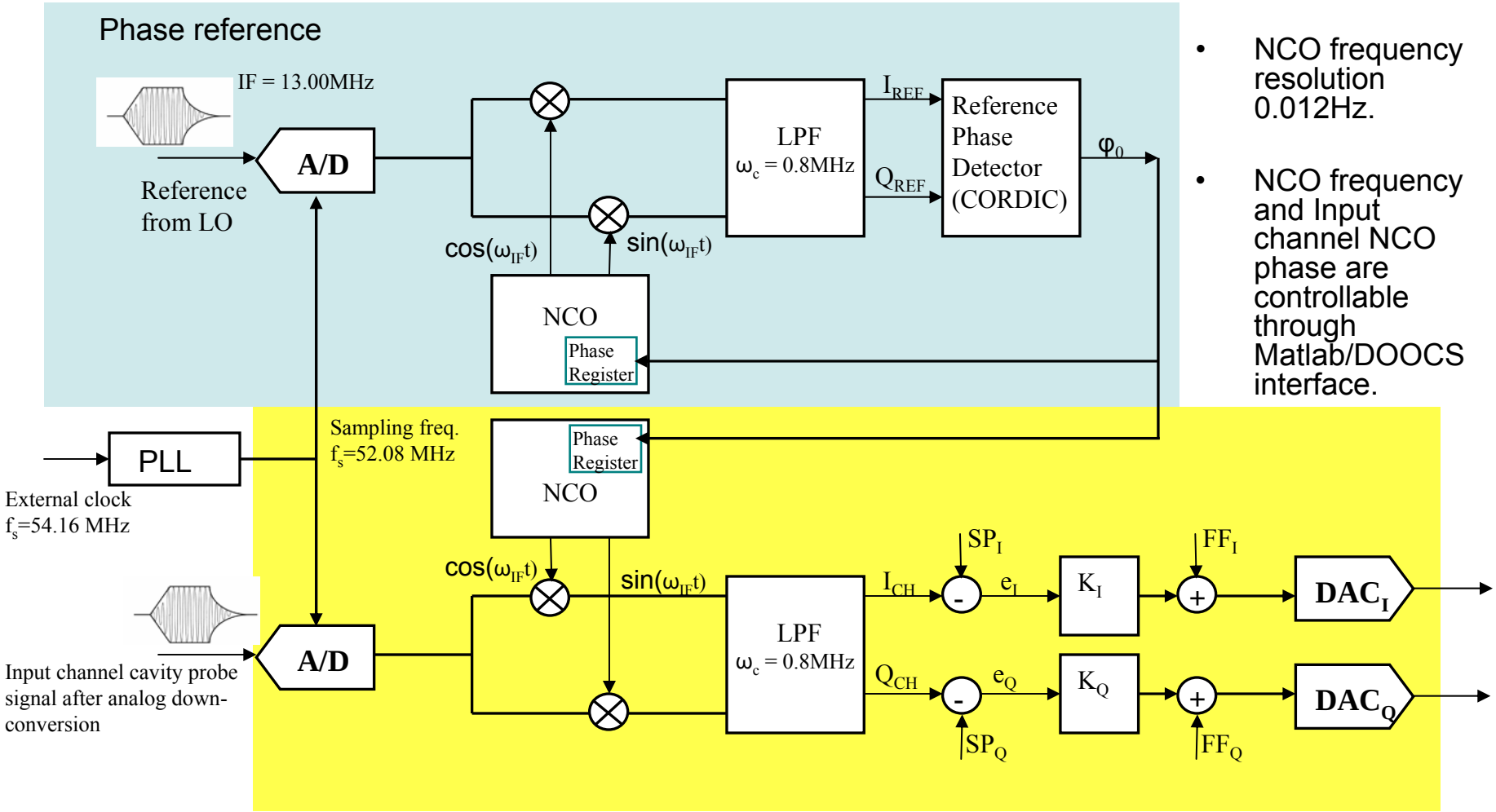
- DAQ and data interface is still based on DESY's DAQ with some modifications.
- The Matlab applications and portions of DOOCS have been migrated to LINUX.



ESECON functions

- DDS with tunable frequency in each input channel.
- Reference channel with automatic phase detector and phase tracking based on the CORDIC algorithm.
- Digital Filtering.
- Cavity field vector-sum.
- PI control.
- Digital Up converter to IF for the drive.
- Most of the firmware has been implemented using the Matlab/Simulink/System-Generator approach.
- Borrowed from Simcon3.1(VHDL)
  - DAQ to capture data.
  - (iid) interface to Matlab and DOOCS servers.

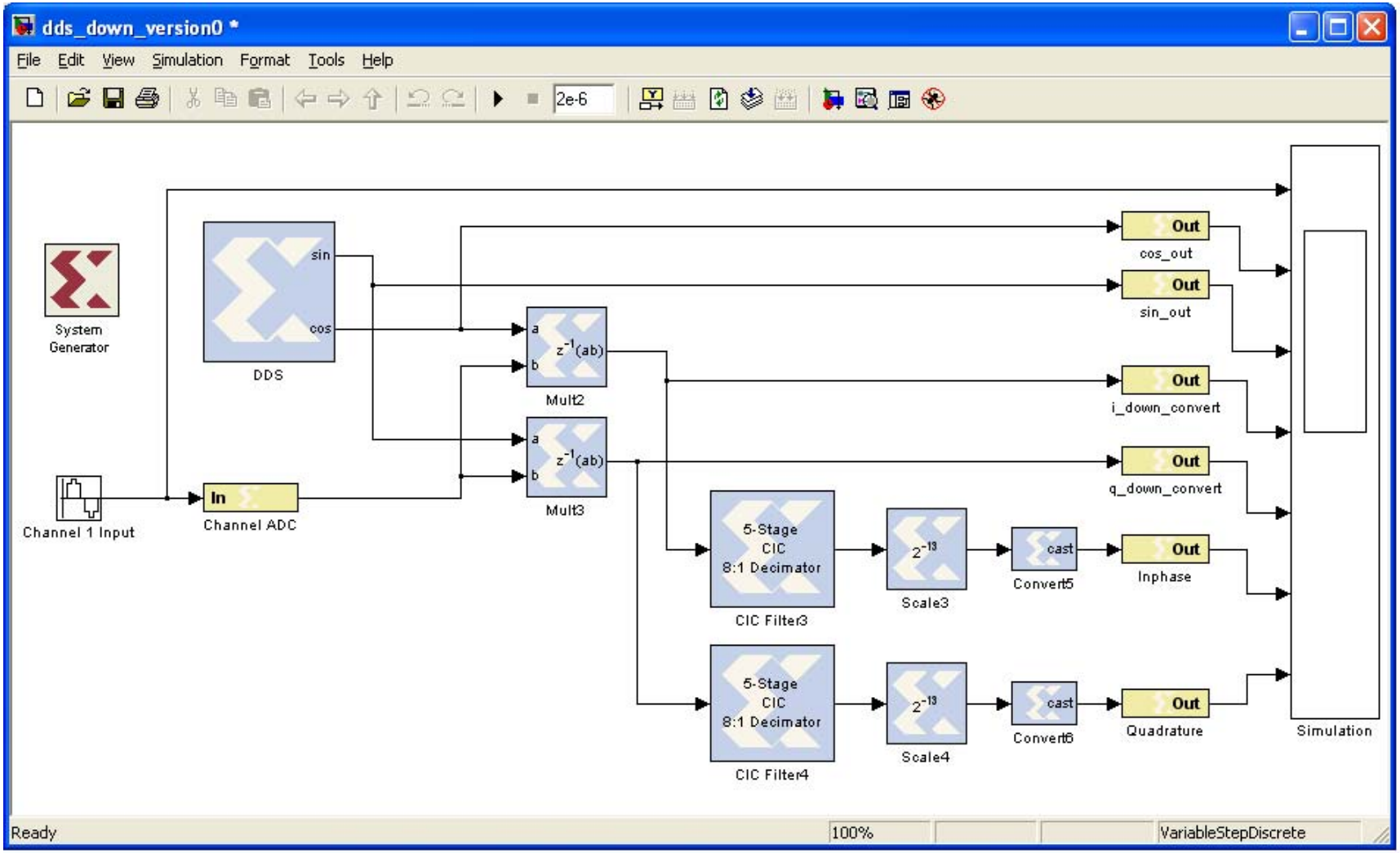
Block diagram of LLRF functions in firmware



- NCO frequency resolution 0.012Hz.
- NCO frequency and Input channel NCO phase are controllable through Matlab/DOOCS interface.

f_{IF}/f_s= 13/50 to keep harmonics and DDC aliases out of the passband.

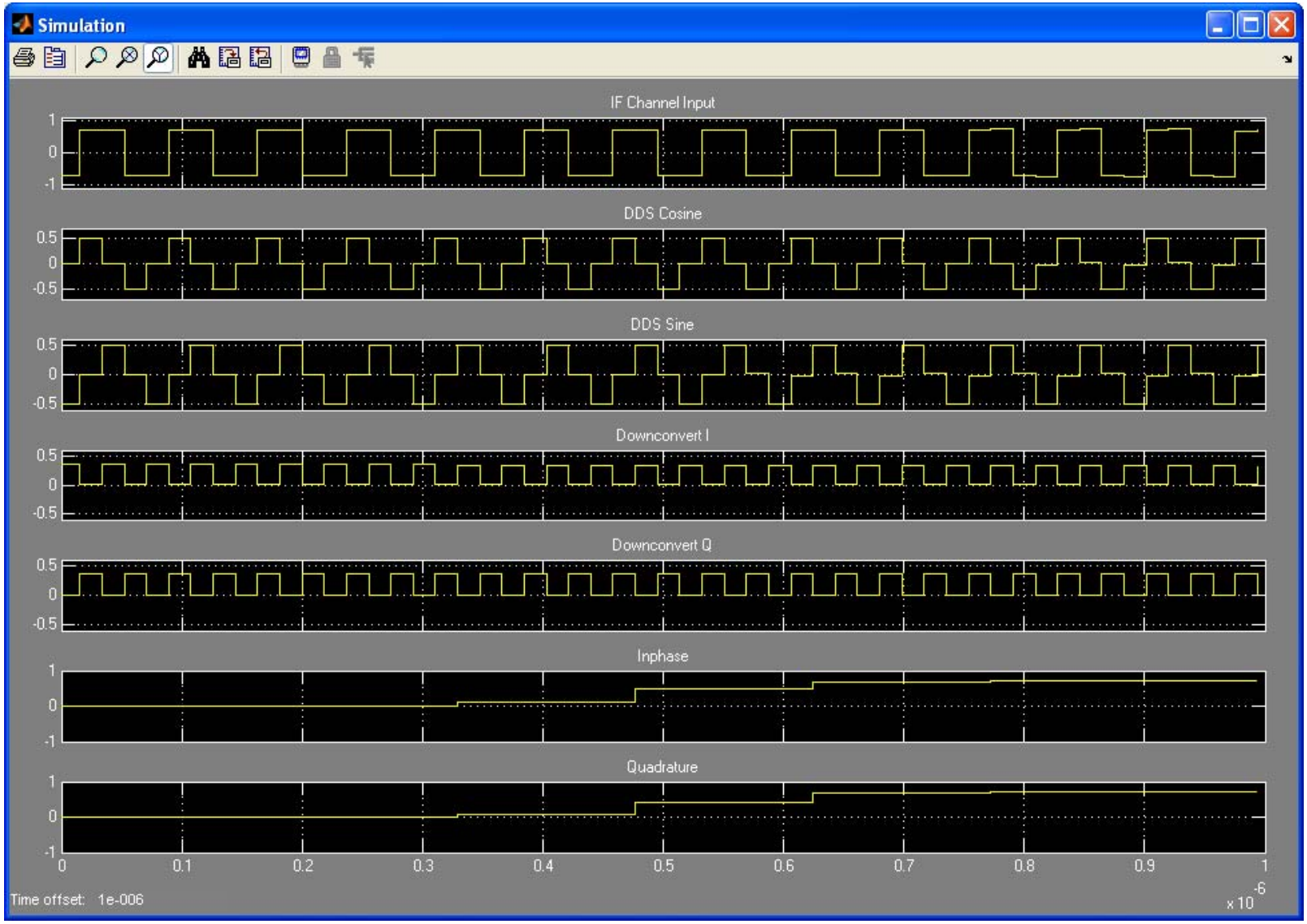
Firmware implementation using Simulink, Matlab and SysGen



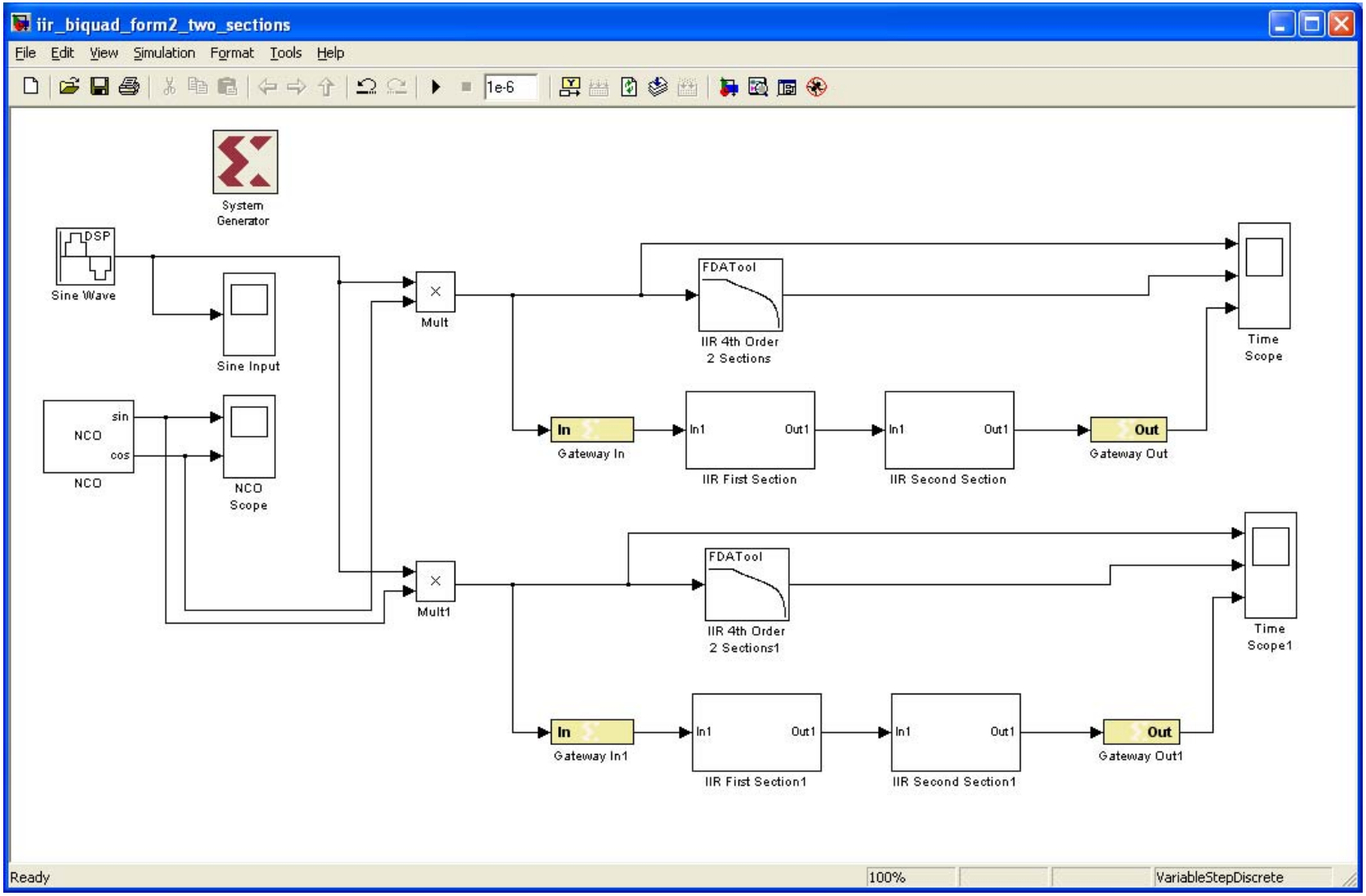
SysGen Intellectual Property (IP) library blocks are optimized for efficient use of FPGA resources

Perform complex functions: With a few IP blocks, an IF signal is downconverted into its I and Q components

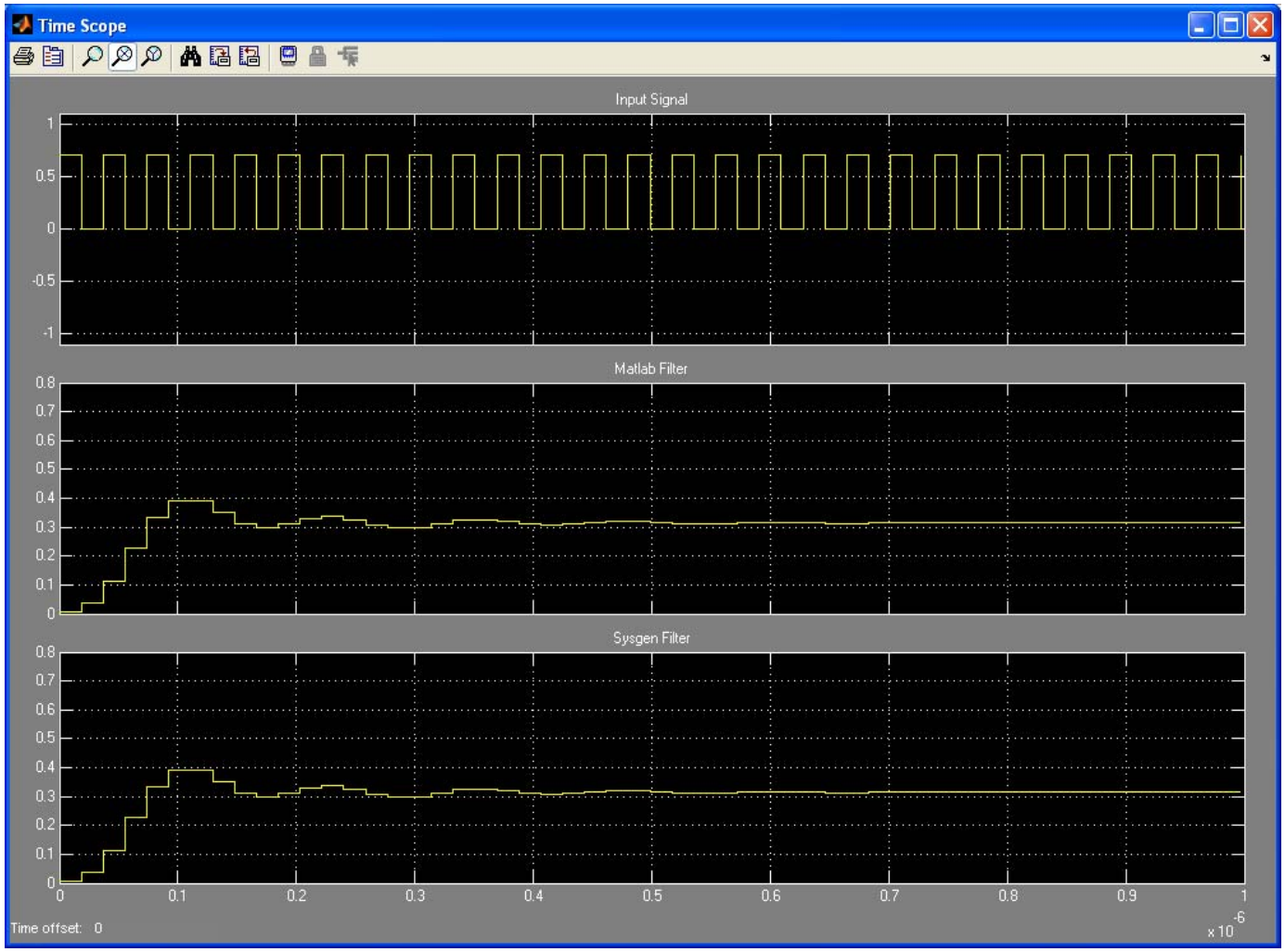
Simulation of signal flow through hardware stages



An IIR filter is designed with Matlab and is then reproduced in System Generator

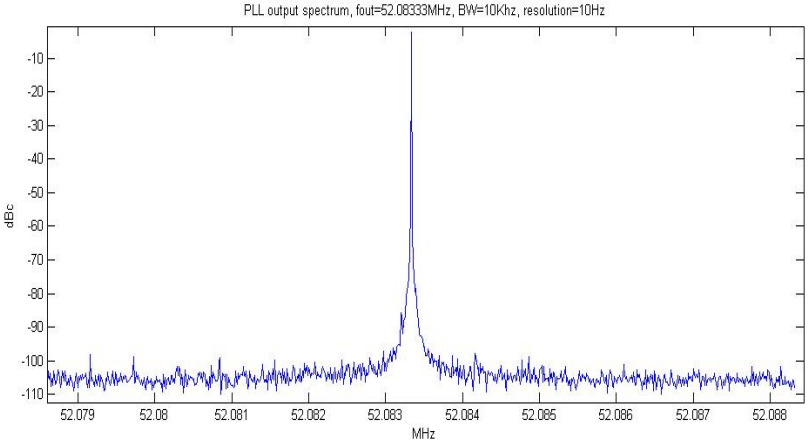


Compare each filter's behavior in the simulation

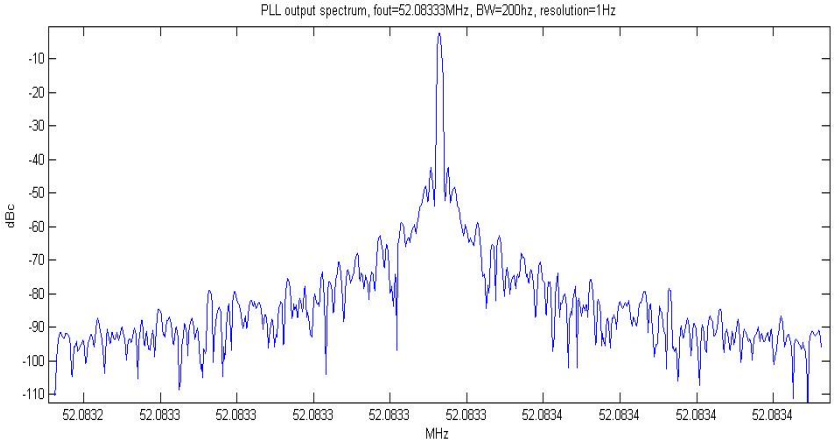


PLL measurements

10KHz span

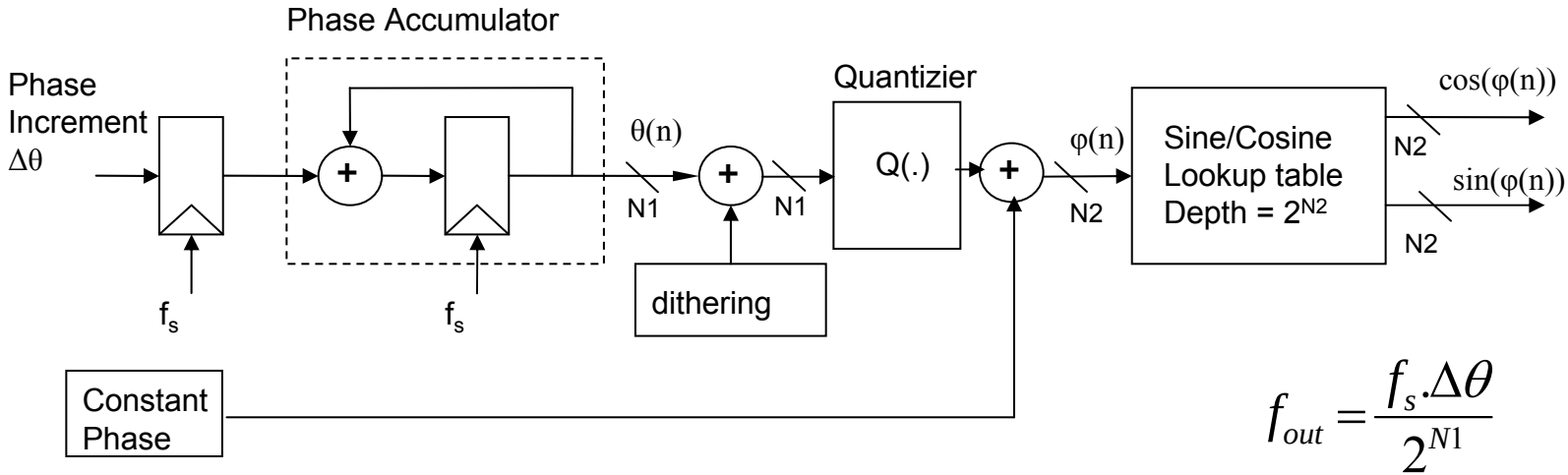


200Hz span



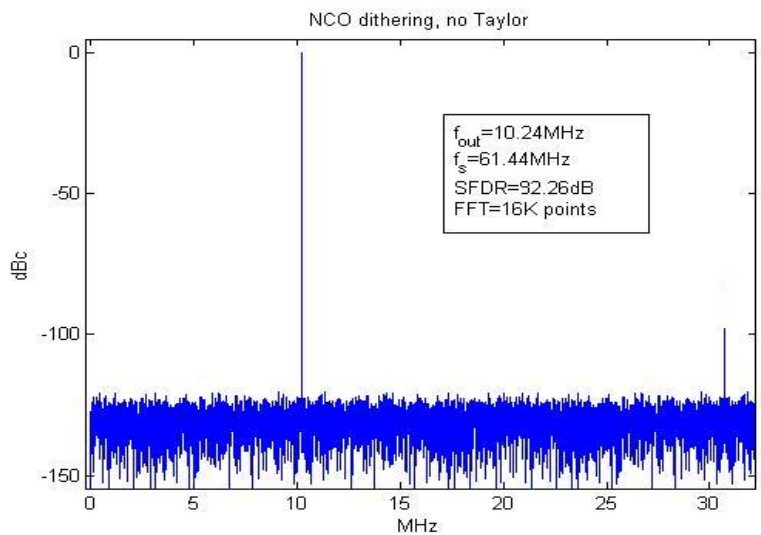
- PLL and clock distribution device is TI cdcm7005.
  - The PLL locks to the external clock coming from the LO distribution.
  - Maximum external clock frequency as PLL input is 125MHz.
  - 2nd production of boards will include the option of using the LO (1313MHz) as external clock bypassing the PLL, and using only the clock dividers.
- Integrated phase jitter (1KHz-10MHz) ~230fs

NCO block diagram (with dithering)



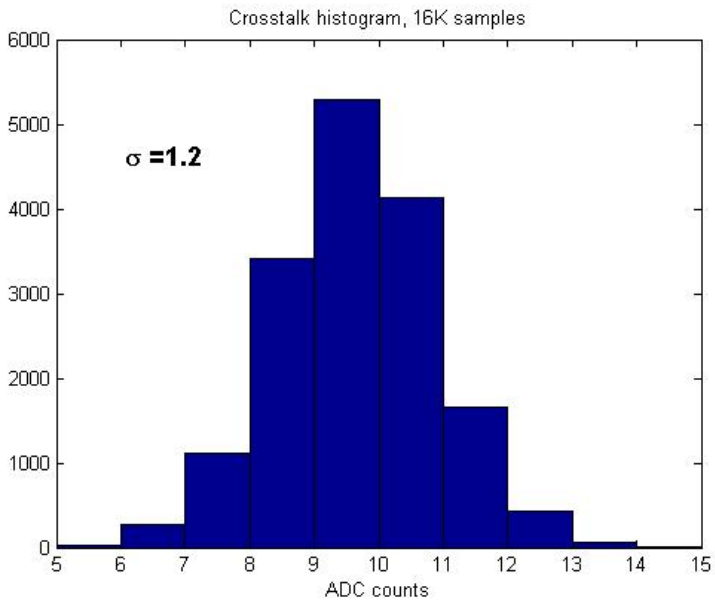
$$f_{out} = \frac{f_s . \Delta\theta}{2^{N1}}$$

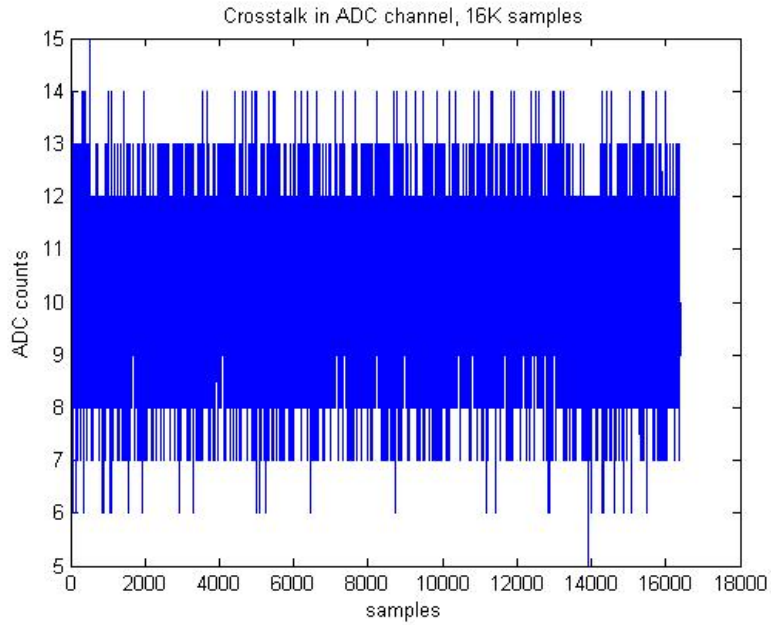
- 32-bit phase accumulator, 12-bit quantizier, 1K-deep LUT.
- NCO provides sin and cosine with tunable output frequency.
  - Frequency resolution 0.0279396Hz.



ADC noise and crosstalk

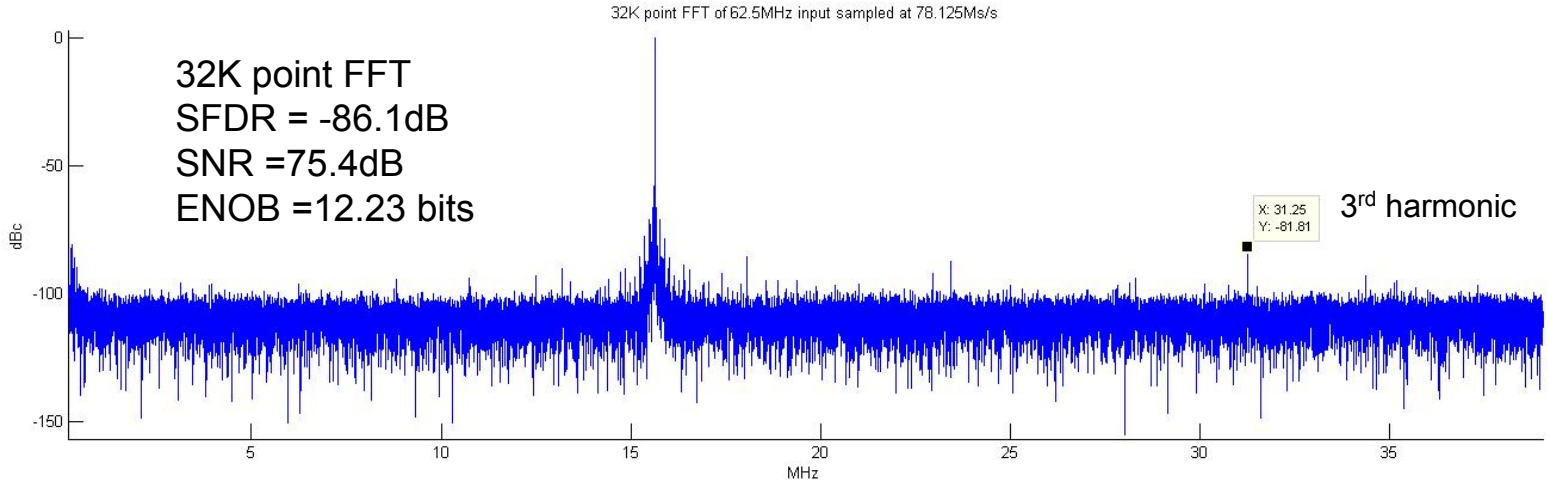
Crosstalk measured using a 50Ω termination in one channel and a 2Vpp square wave signal in a neighboring channel. There are 2 channels per ADC. So, both channels are connected to the same device.



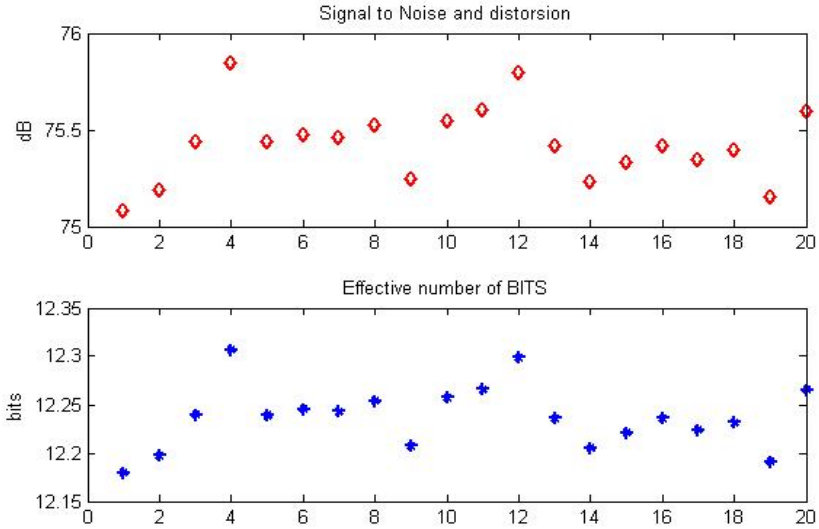


Sampling frequency is 78.125 MHz

Single tone FFT

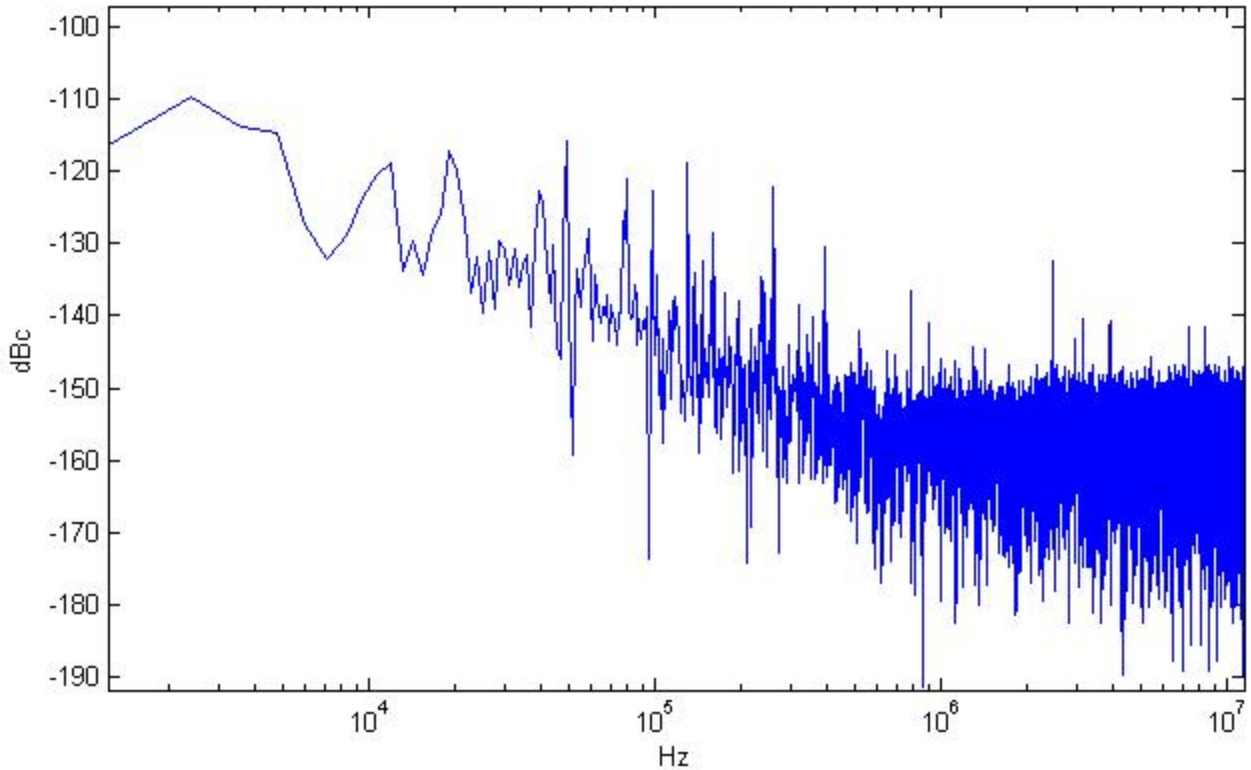


Data sample using from 4 different ADC channels



ADC phase noise

ADC phase noise at zero crossing. f_s=78.125MHz, f_{in}=62.5MHz



This plot does not have enough resolution to clearly see the close in noise.

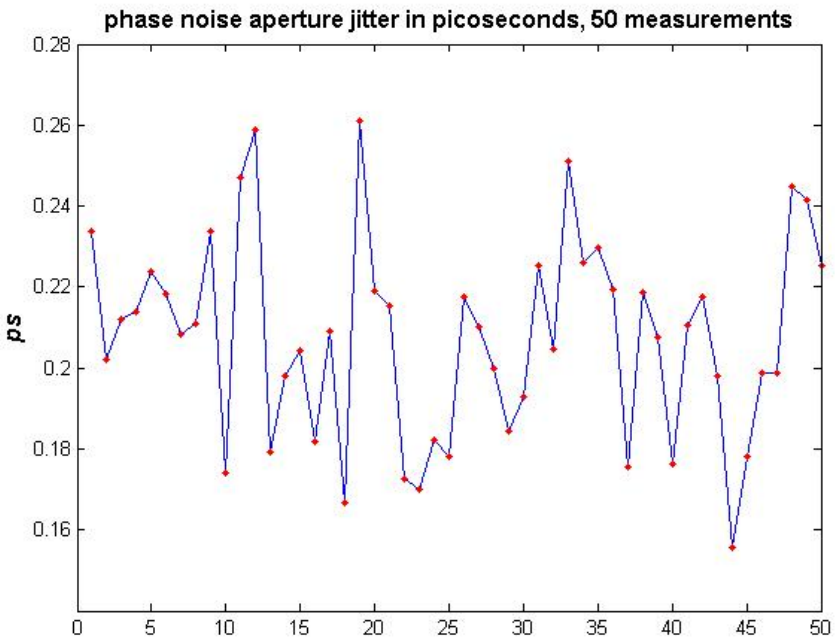
Phase jitter

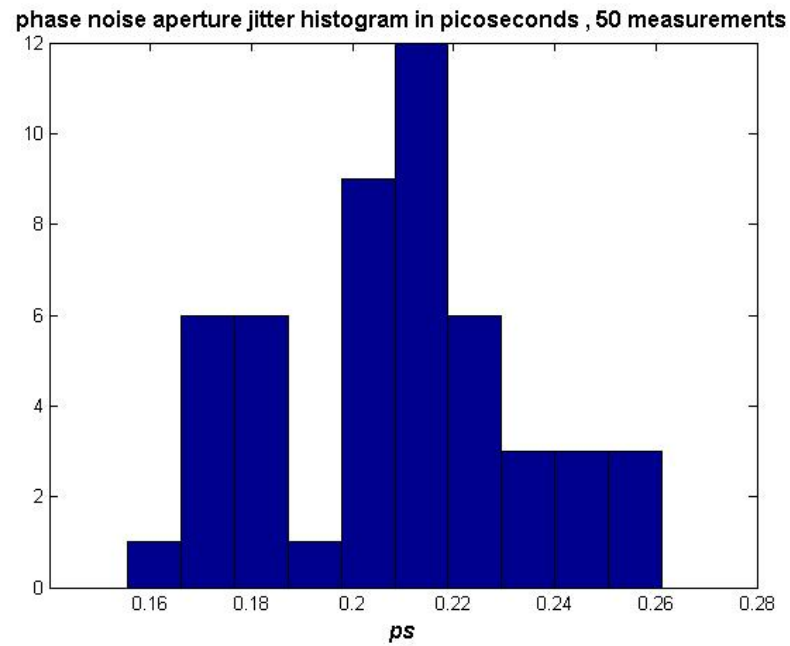
Procedure:

- Measure SNR using a low frequency input (3MHz)
- Measure SNR using a high frequency input (62.5MHz)
- Calculate jitter measured by aperture time in ps.

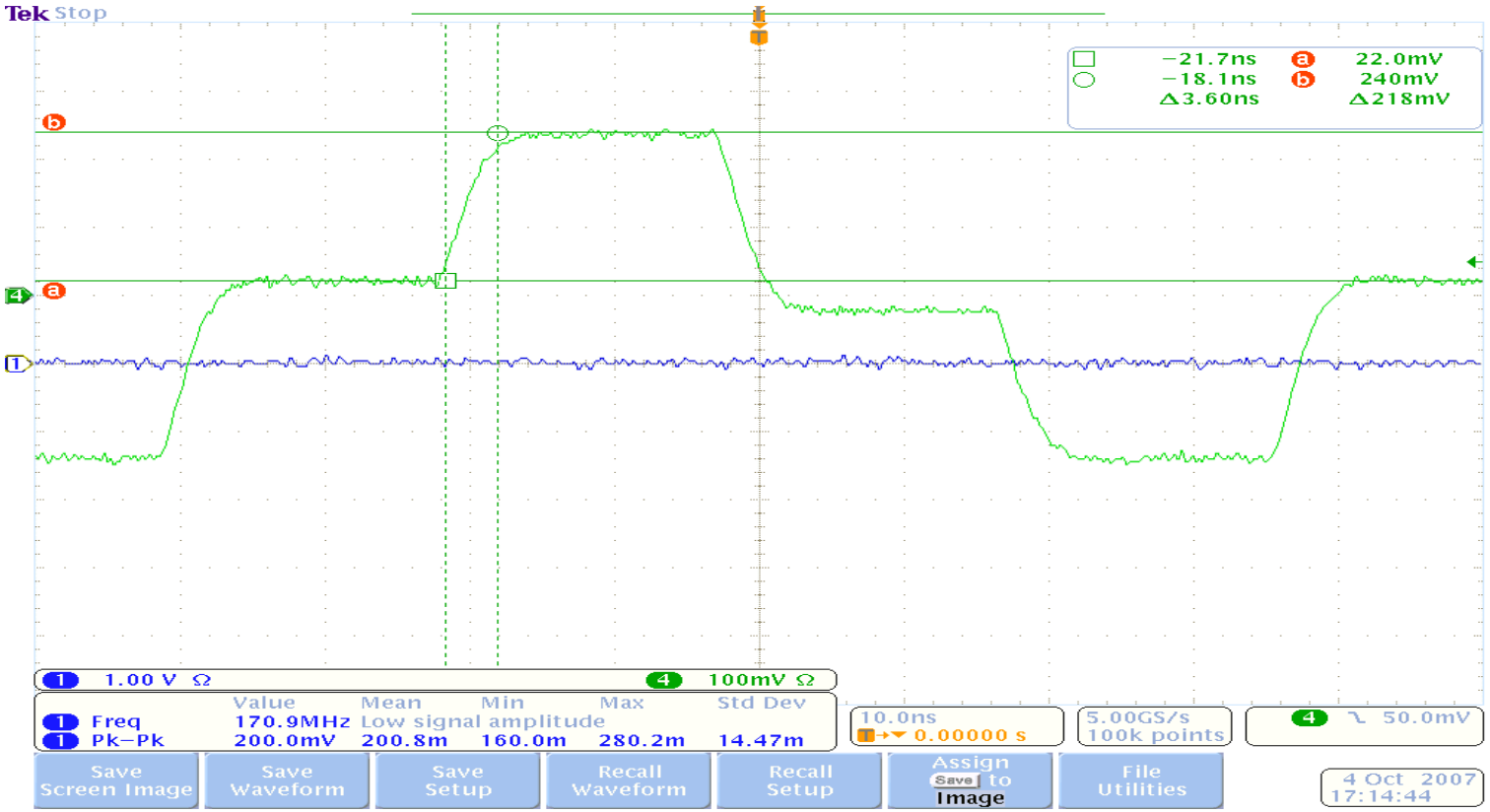
$$SNR = -20 * \log\left[(2\pi t_a)^2 + \left(\frac{1+\varepsilon}{2^N}\right)^2\right]^{1/2}$$

$$t_a = \frac{\sqrt{\left(10^{-SNR/20}\right)^2 - \left(\frac{1+\varepsilon}{2^N}\right)^2}}{2\pi f}$$



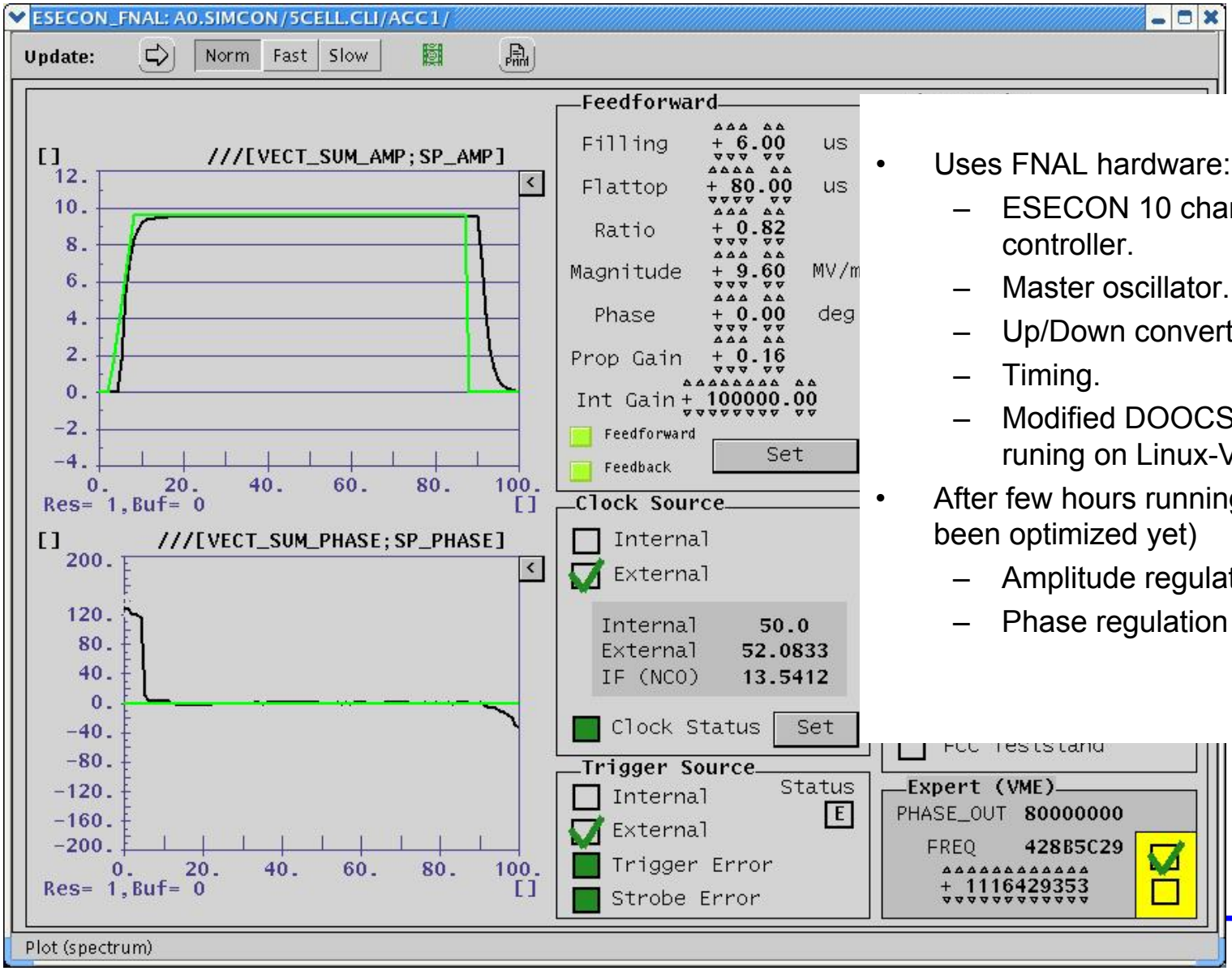


DAC performance



- DAC rise time 3ns

3.9 GHz deflecting mode Cu cavity (FNAL photo-injector)



- Uses FNAL hardware:
  - ESECON 10 channel LLRF controller.
  - Master oscillator.
  - Up/Down converters.
  - Timing.
  - Modified DOOCS server and GUIs runing on Linux-VME.
- After few hours running, (system has not been optimized yet)
  - Amplitude regulation of 0.1% rms.
  - Phase regulation of 0.05º rms.

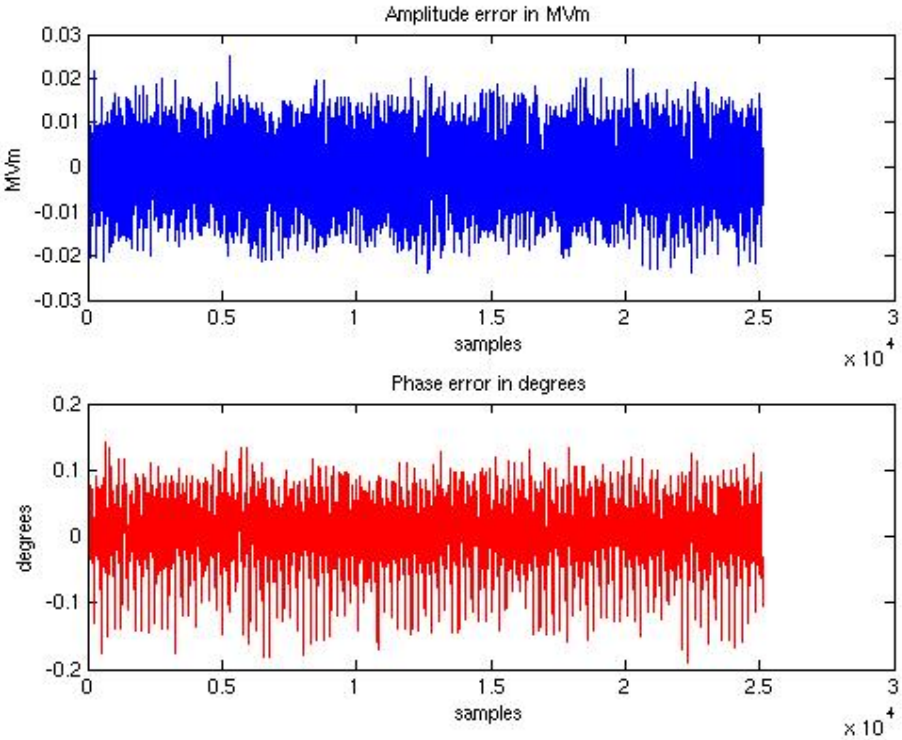
LLRF tests at DESY-FLASH, Sept. 14-17 2007

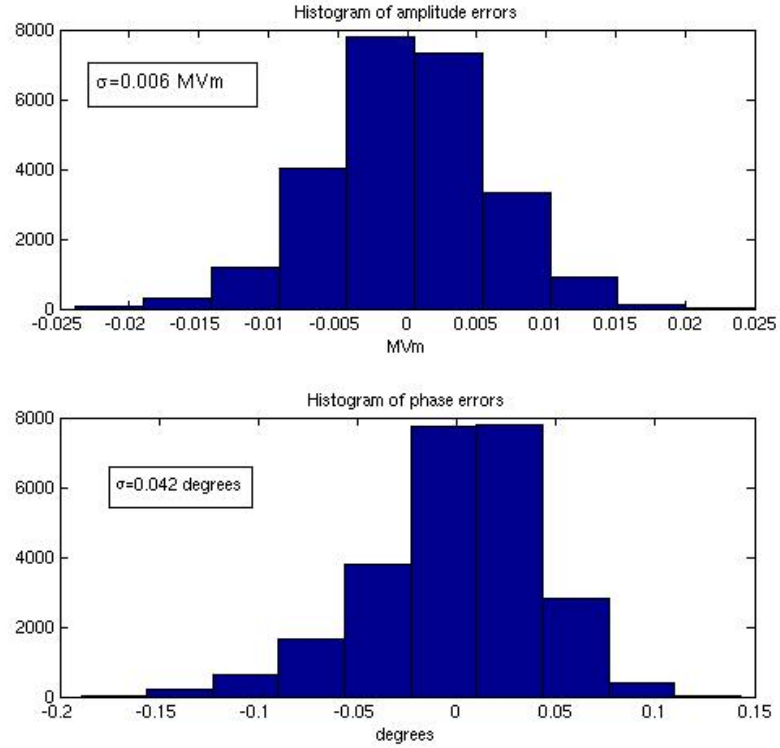
- Tests were carried out in the FLASH injector (Cryomodule 1). FNAL Hardware, firmware and software used:
  - Master oscillator, 8 channel down-converter, 10 channel controller (ESECON).
  - DDC, filters, controller, DUC firmware.
  - VME-linux software, data analysis scripts for Matlab.

- Test conditions:
  - VS at 15 Mv/m.
  - Beam: 30 bunches.

- Measurements:
  - FNAL-LLRF system noise characterization.
  - FF and closed loop cryomodule control.

LLRF tests at DESY-FLASH, Sept. 14-17 2007

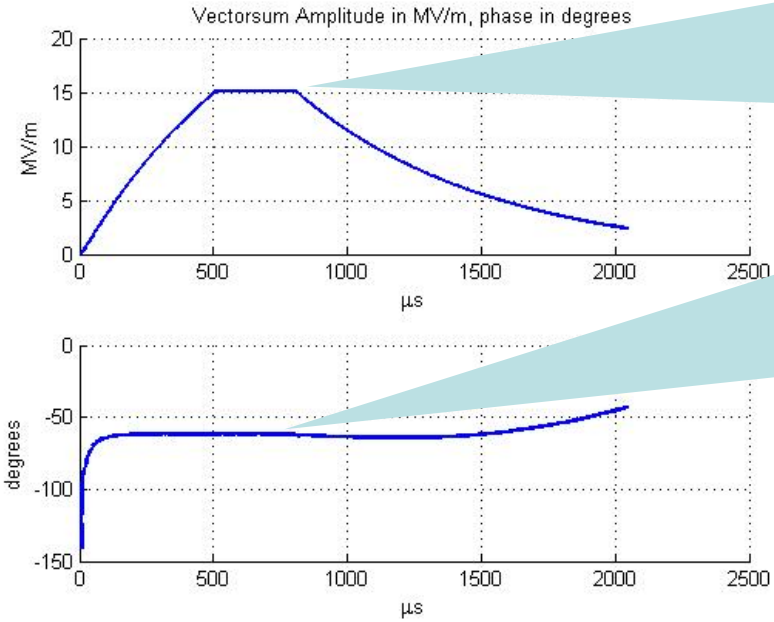


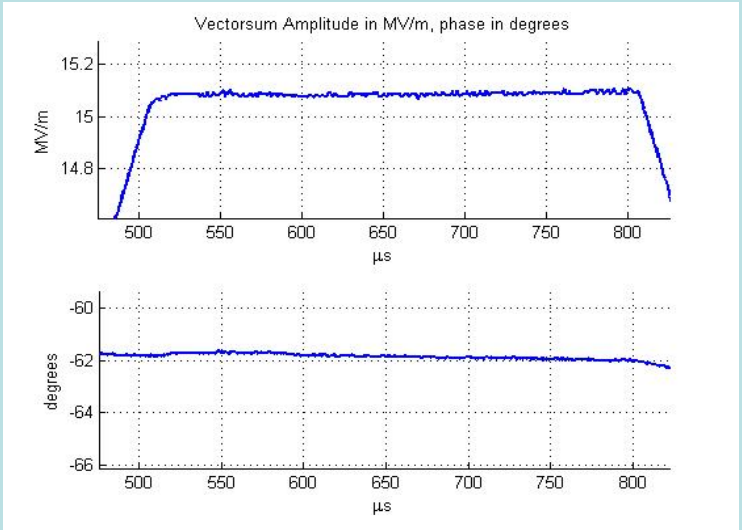


- The noise in the FNAL-LLRF system was measured using existing cavity probe splits while the existing DESY LLRF was controlling the cryomodule.
- RMS error:
  - Amplitude noise: 1.88e-4 (SNR=74.5dB).
  - Phase: 0.042 degrees.

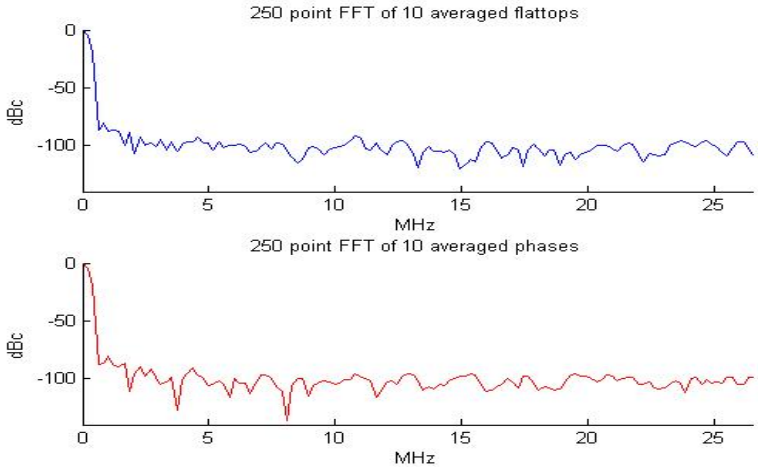
LLRF tests at DESY-FLASH, Sept. 14-17 2007

Closed loop gain of 40 before 8/9 π mode and group delay started unstabilizing the loop





Amplitude and phase FFTs during the RF pulse flattop



Summary

- FNAL hardware is starting to work well.
  - Room for fine tuning and optimization.
  - Single cavity systems are being commissioned.
  - We have basic hardware to start working with the first cryomodule at NML.
  - Now the effort has to be focused on algorithms and software.
    - Control interface.
    - Automation
- Hopefully very soon we will have a system that can be used in the RF R&D program.

Thanks for your attention.